A 4.25-Gbps Transmitter Optical Sub-Assembly (TOSA) Using an 850-nm Vertical-Cavity Surface-Emitting Laser (VCSEL)

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ABSTRACT The explosive growth of the Internet in recent years has given rise to a need for higher data transmission speeds. And the rapid proliferation of electronic appliances raises the hope for greater proliferation of short-haul data communications linking various appliances in the home. Against this background an 850-nm vertical-cavity surface-emitting laser (VCSEL) transmitter optical sub-assembly (TOSA), which can operate at 4.25 Gbps, is the target of R&D activity in institutions around the world as a light source for the next generation of Fiber Channel. Accordingly we have optimized the structure of a VCSEL chip, fabricated a TOSA, and evaluated its characteristics. This has enabled us to fully satisfy specifications with respect to 4.25-Gbps operation, static characteristics, temperature characteristics, and reliability.

1. INTRODUCTION

The explosive growth of the Internet in recent years has given rise to a need for higher data transmission speeds. And the rapid proliferation of electronic appliances raises the hope for greater proliferation of short-haul data communications linking various appliances in the home.

The 850-nm vertical-cavity surface-emitting laser (VCSEL) [1] chip is already being used in a transmitter optical sub-assembly (TOSA), as a driver for gigabit Ethernet or Fiber Channel data communications applications.

At present VCSEL TOSAs are mainly used at transmission speeds of 2.5 Gbps or less, but there is a strong movement toward increasing Fiber Channel speed to 4.25 Gbps, creating the need for a VCSEL TOSA capable of 4.25-Gbps operation.

We have therefore fabricated an 850-nm VCSEL TOSA capable of 4.25-Gbps operation, and have evaluated its operation at 4.25 Gbps, together with its static characteristics, temperature characteristics and reliability. As a result we have obtained characteristics that fully satisfy specifications, as reported in the following.

2. VCSEL CHIP STRUCTURE AND ITS OPTIMIZATION

TOSA characteristics, except for high-frequency modulation characteristics, are almost entirely determined by the characteristics of the VCSEL chip. In this section we discuss the structure of an 850-nm VCSEL chip, and the optimization of its design.

2.1 Structure of the VCSEL

In the oxide-confined structure [2] developed in the work described here, the effective confining of current and light by means of an aluminum oxide layer has resulted in the achievement of outstanding characteristics in terms of threshold current, high efficiency [3), 4)], etc.

What is more, the L/I (optical power/current) and V/I (voltage/current) characteristics are heavily dependent on the diameter of the light-emitting region (oxide aperture size) enclosed by the aluminum oxide layer referred to. This means that it is possible to achieve the desired characteristics by controlling the oxide aperture size.

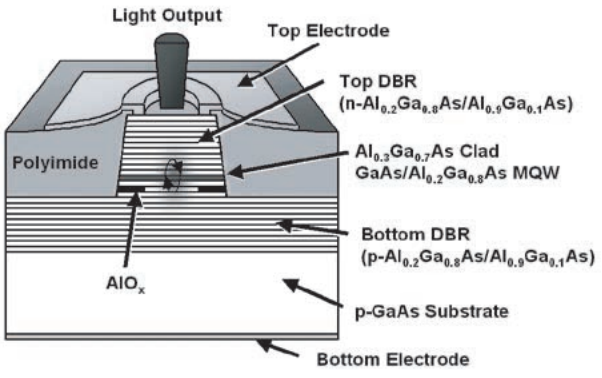

Figure 1 Structural schematic of oxide-confined VCSEL.

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Figure 1 is a schematic diagram showing a cross-section of an 850-nm oxide-confined VCSEL [5]. This structure consists of a p-type GaAs substrate onto which are grown a bottom distributed Bragg reflector (DBR) mirror comprising 35 pairs of p-type $Al_{0.2}Ga_{0.8}As/Al_{0.9}Ga_{0.1}As$, an active layer ($\lambda$ cavity) comprising a $GaAs/Al_{0.2}Ga_{0.8}As$ multiquantum well (MQW), and a top DBR mirror comprising 25 pairs of n-type $Al_{0.2}Ga_{0.8}As/Al_{0.9}Ga_{0.1}As$. On the low refraction index layer closest to the active layer in the bottom DBR mirror there is formed an AlAs layer (aluminum oxide layer formed by wet oxidation) for the purpose of confining current and light. Further, a pad electrode is formed on the polyimide for reducing parasitic capacitance.

In this work we have fabricated chips with different oxide aperture sizes and evaluated their various characteristics, effecting the optimization of chip structure (oxide aperture size).

2.2 Optimizing the VCSEL Structure

Table 1 shows some of the specification of a 4.25-Gbps VCSEL TOSA. In this work, from among a number of characteristics, we report on two that are of the utmost importance in transceiver design and are in a trade-off relationship with oxide aperture size: threshold current and differential resistance. Measurements were taken in the wafer state at 25°C using DC drive. We also report on the temperature dependence of threshold current, lasing wavelength, slope efficiency and differential resistance.

Finally, although the importance of chip characteristics are as assembled in the TOSA, it was found that there was virtually no difference between the characteristics of the chip itself and those when assembled into the TOSA, so in this work we effected the optimization in the chip state.

Figure 2, plotting oxide aperture size dependence of threshold current, shows a substantially linear relationship. It can be seen that to satisfy the TOSA specifications in Table 1, it is sufficient to set the oxide aperture size at 130 μm^2 or less.

Similarly Figure 3 shows the results for differential resistance, which is in inverse proportion to oxide aperture size. It can be seen that to satisfy the TOSA specifications in Table 1, it is sufficient to set the oxide aperture size in the range of 60 to 120 μm^2.

Let us now proceed to discuss results for temperature characteristics. The temperature dependence of threshold current, lasing wavelength, slope efficiency and differential resistance are shown in Figures 4 through 7 respectively. Measurements were taken in the wafer state at temperatures of from 20 to 70°C using DC drive.

This resulted in a fluctuation in threshold current of ± 0.2 mA, temperature dependence of lasing wavelength of 0.59 nm/°C, temperature dependence of slope efficiency of −3300 ppm/°C, and temperature dependence of differ-

Table 1 Specification of 4.25-Gbps VCSEL TOSA.

Item	Min.	Max.
Threshold current (mA)	—	2.5
Differential resistance (Ω)	25	50
Temperature dependence of threshold current (mA)	−1	+1
Temperature dependence of wavelength (nm/°C)	—	0.07
Temperature dependence of slope efficiency (ppm/°C)	—	−4500
Temperature dependence of differential resistance (ppm/°C)	—	−3000

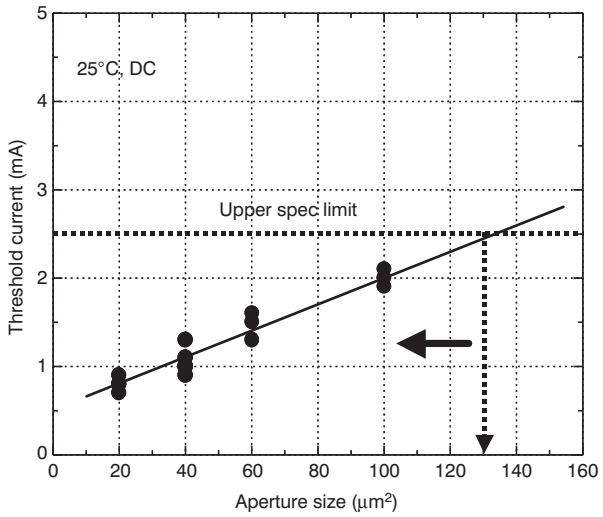

Figure 2 Oxide aperture size dependence of threshold current.

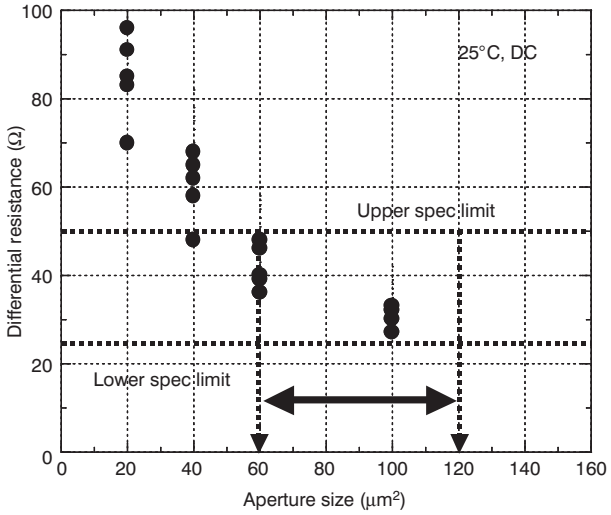

Figure 3 Oxide aperture size dependence of differential resistance.

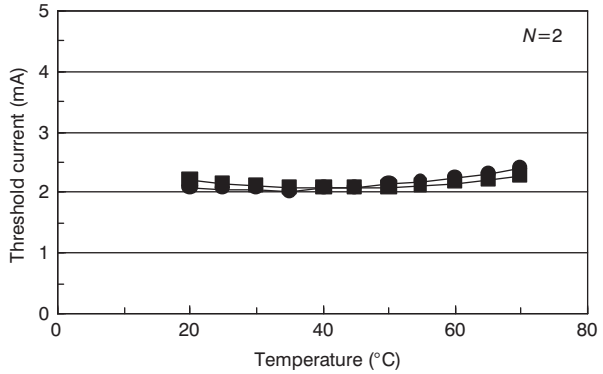

Figure 4 Temperature dependence of threshold current.

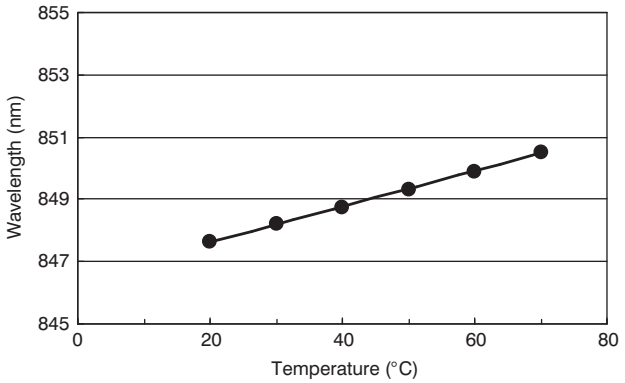

Figure 5 Temperature dependence of lasing wavelength.

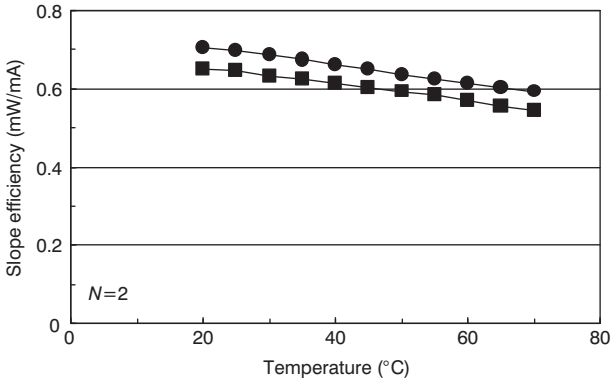

Figure 6 Temperature dependence of slope efficiency.

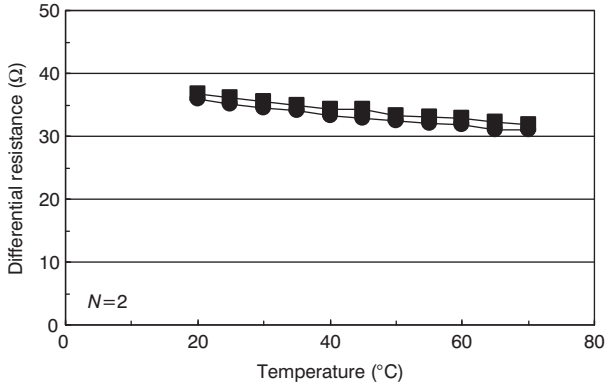

Figure 7 Temperature dependence of differential resistance.

ential resistance of −2500 ppm/°C, confirming that for all these characteristics the specifications shown in Table 1 were satisfied.

3. 4.25-GBPS VCSEL TOSA

At present TOSAs with speeds of 2.5 Gbps are the mainstay of the market, but in the future this can be expected to shift rapidly to 4.25 Gbps (Fiber Channel standard). Accordingly we proceeded with development work aimed at a maximum modulation speed of 4.25 Gbps or more. In this section we report on the structure of the TOSA, and on the results of evaluation of static characteristics, temperature characteristics, modulation characteristics, eye pattern and reliability.

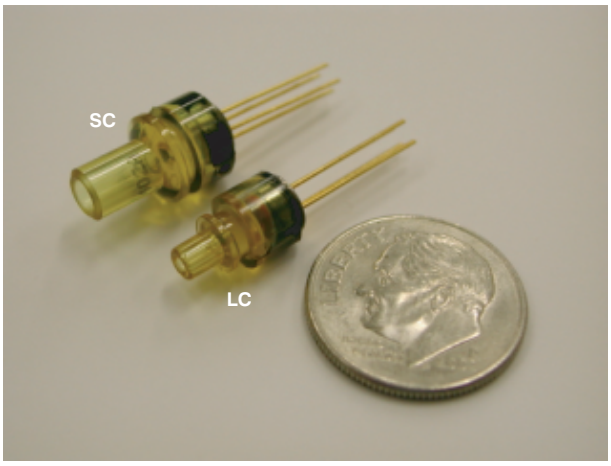

Figure 8 Photograph of 4.25-Gbps TOSAs using 850-nm VCSEL with U.S. 10-cent coin for scale.

3.1 TOSA Structure

Figure 8 shows photographs of the TOSAs developed in this work, that with the SC barrel at top left and LC barrel at bottom right. Normally in the 850-nm band multimode fibers with a core diameter of 50 or 62.5 μm are used—larger than single-mode fibers (diameter 7 μm), so that coupling is easier. For this reason plastic barrels are used at fiber couplings. Monitor photodiodes are incorporated to enable auto power control (APC) drive. The VCSEL chip is mounted to a TO-46 header via a submount. And since the U.S. Food and Drug Administration specifies that lasers of 850-nm-band wavelengths be used at an eye safety level of Class 1 or below, this structure can be used at an optical power (fiber-coupled) of not more than 350 μW.

3.2 Results of TOSA Evaluation

3.2.1 Static Characteristics

Figure 9 shows the current dependence of optical power, voltage and monitor current at 25°C, DC drive. Threshold current was 1.8 mA, optical power was 450 μW @6 mA (coupling efficiency with GI-50 multimode fiber of approximately 70%, so that fiber coupling power was 300 μW), operating voltage was 1.9 V @6 mA, differential resistance was 40Ω @6 mA, and monitor current was 400 μA @6 mA, fully satisfying specifications.

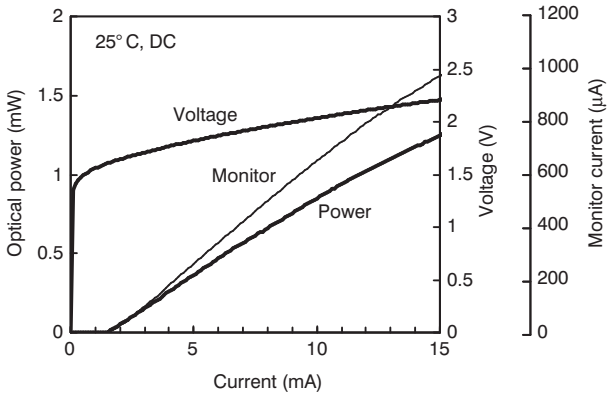

Figure 9 Current dependence of optical power, voltage and monitor current.

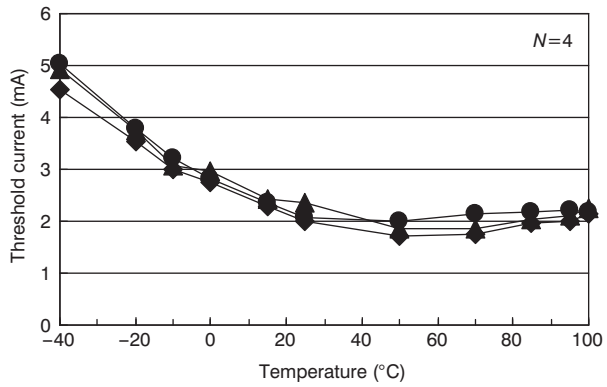

Figure 10 Temperature dependence of threshold current.

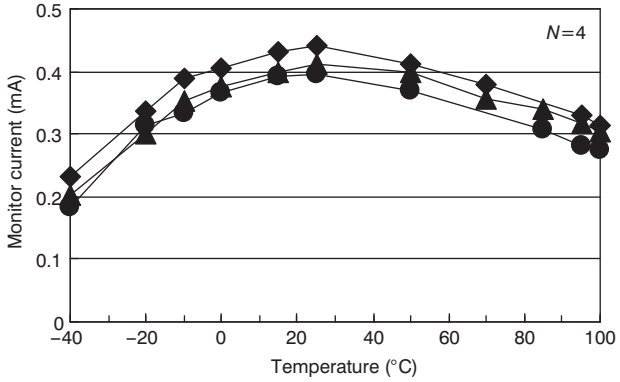

Figure 11 Temperature dependence of monitor current.

3.2.2 Temperature Characteristics

In a transceiver for a data storage area network (SAN), Fiber Channel standards are mainly used, with the operating temperature range specified at 0 to 70°C. When the temperature rise inside the transceiver is taken into account, the TOSA mounted in such a transceiver must deliver stable operation from 0 to 80°C. And depending on the application, even more severe conditions must be contemplated—temperatures of from −40 to 95°C. Accordingly in this work we evaluated temperature characteristics over a wide range— −40 to 100°C. Figures 10 and 11 show the temperature dependence of threshold current and monitor current.

The amount of fluctuation in threshold current with respect to temperatures of 0 to 80°C (the Fiber Channel standard value), which was the main target in this work, was extremely small—only ±0.2 mA, which fully satisfied the specification (±1 mA). At the lower end of the −40 to 100°C temperature range (−10°C or below), however, the rise in threshold current had an effect and the fluctuation in threshold current was ±1.5 mA, greater than the specification. This is because of the large value of detuning, as determined by the difference between the gain peak wavelength and the Fabry-Perot wavelength (because of the optimized design for the 0 to 80°C range), making possible appropriate adjustment by means of design.

The fluctuation in monitor current was also very low—only 0.1 %/°C—fully complying with the specification of 0.3 %/°C.

Further, in terms of the temperature dependence of lasing wavelength, slope efficiency and differential resistance, the measurement results were substantially similar to those for the chip.

3.2.3 Modulation Characteristics

As a result of the influence of wire inductance, and the inductance and capacitance of the TO header itself, the modulation bandwidth when assembled in the TOSA configuration is more restricted in comparison with the frequency characteristics of the chip alone. Specifically, this influence becomes suddenly apparent if modulation speed exceeds 2.0 GHz. Since the f_{3dB} band for the VCSEL chip developed here is approximately 8 GHz, 4.25-Gbps operation presents no problem for the chip by itself, but the effect due to the assembling referred to above imposes restrictions on the modulation bandwidth.

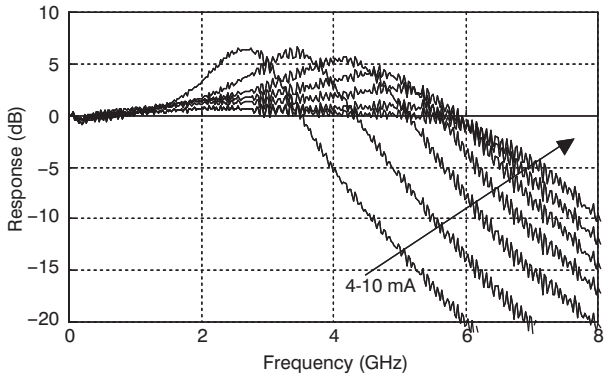

Figure 12 Small-signal modulation characteristics.

Figure 12 shows the result of measurements of small-signal modulation characteristics. It can be seen that at bias currents of 5 mA or less the resonance peak of relaxation oscillation is below 4 GHz, raising concerns about influence on the eye pattern.

At bias currents in excess of 6 mA, on the other hand, relaxation oscillation frequency obtained is higher than 4 GHz, and for the f_{3dB} band is higher than 5 GHz. These results are comfortably clear of the 3.0 GHz theoretically required for 4.25-Gbps operation. Since the threshold current of the chip used in these measurements is 1.8 mA, we may estimate that to achieve 4.25-Gbps operation would require a normalized bias level [bias current − threshold current]/threshold current of approximately 2.3 or more.

3.2.4 Eye Patterns

In actual operation in a transceiver, importance attaches to rise time, fall time and jitter in the eye pattern. These characteristics are greatly modified by the circuitry used for mounting in the transceiver, and by the driver IC used to drive the VCSEL. Since the circuitry used in the transceiver, driver IC, etc. will differ according to the designs of each individual customer, the method used here for evaluation was a standard method using a pseudorandom bit sequence (PRBS) from a pulse pattern generator. In order to minimize the effect of inductance from the TO header pins during measurement, the TOSA were soldered onto micro striplines with the pins cut short.

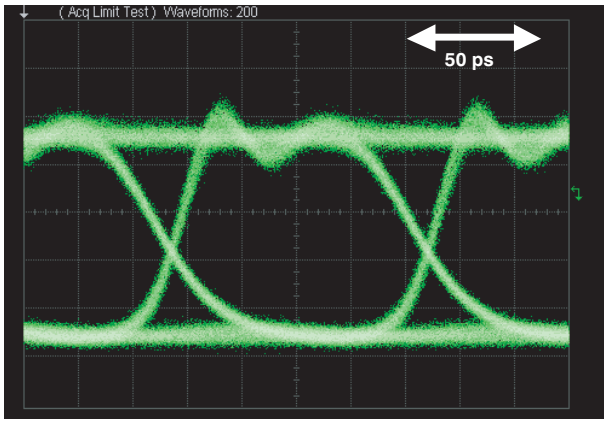

Figure 13 Eye pattern diagram at 4.25 Gbps (extinction ratio 10 dB).

Figure 13 shows the results of measurements of eye patterns with a 4.25-Gbps PRBS ($2^{31}-1$). The operating conditions were: bias current of 6 mA, extinction ratio of 10 dB, and a modulation voltage of 0.5 V, with measurements taken at room temperature without a filter.

Despite the facts that the measurements were made under optimal conditions rather than actual service conditions, they yielded excellent results—rise and fall times (20~80 %) of 38 ps and 70 ps respectively and jitter of 20 ps or less—fully satisfying the specifications of 90 ps for rise time and 90 ps for fall time.

Let us now discuss the temperature dependence of rise time, fall time and jitter as found from the results of temperature dependence for the 4.25-Gbps PRBS ($2^{31}-1$) eye pattern. These are shown for temperatures of −40 through 100°C in Figures 14 through 16. The measurements were taken at an extinction ratio of 10 dB, modulation voltage of 0.5 V, optical power fiber output of 300 μW constant (APC control).

The result was that at temperatures from 0 to 80°C (0~70°C for the transceiver itself and assuming an internal temperature rise of 10°C) the Fiber Channel standards were a rise time of 35~40 ps, fall time of 40~100 ps and jitter of 18~22 ps. Even when the temperature range was broadened (−40 to 100°C), the maximum values were 40 ps for rise time, 78 ps for fall time and 24 ps for jitter, confirming that at a temperature range of −40 to 100°C the specifications were fully satisfied.

But since, as has been explained above, matching with transceiver circuitry and the driver IC is important in actual use, it is essential in the last analysis that evaluation be conducted on chips mounted in transceivers.

3.2.5 Reliability

Any discussion of reliability must be broadly classified in terms of random failure or wear-out failure; but here we report on the role of wear-out failure. Figure 17 shows the results of a 5000-hr high-temperature aging test of VCSEL chips. Figure 18 shows the results of a 2000-hr high-temperature aging test of of a 4.25-Gbps VCSEL TOSA. The test conditions were a temperature of 100°C, operating current density of 10 kA/cm^2 and automatic

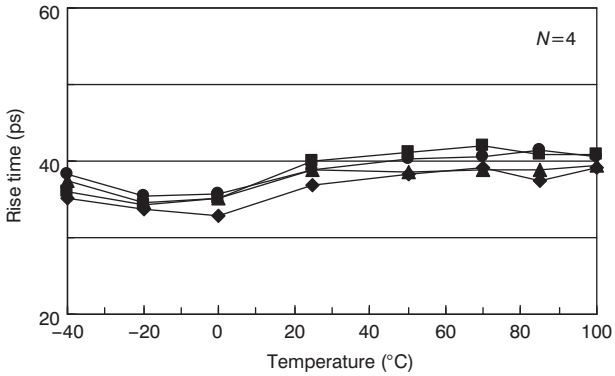

Figure 14 Temperature dependence of rise time.

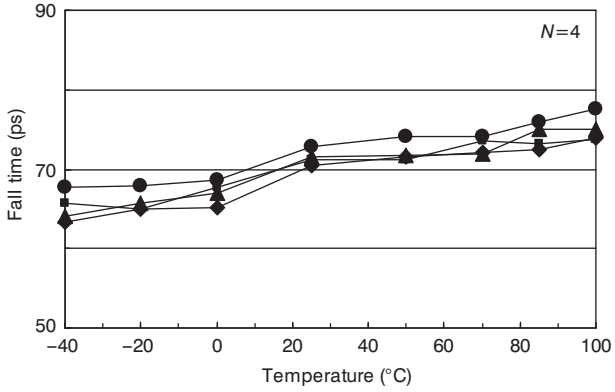

Figure 15 Temperature dependence of fall time.

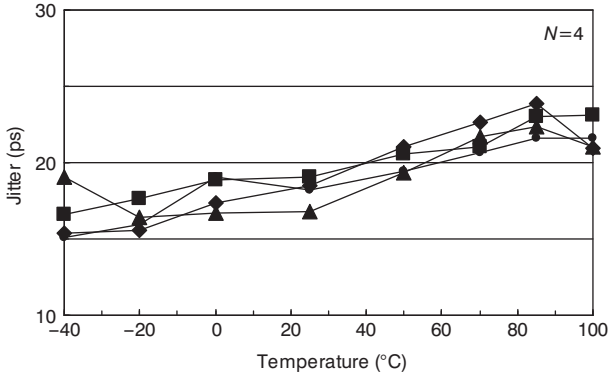

Figure 16 Temperature dependence of jitter.

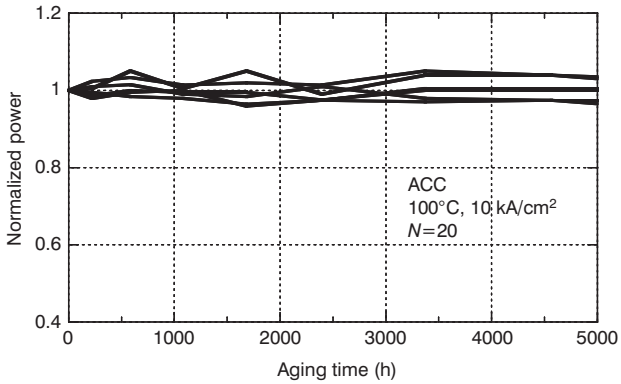

Figure 17 Results of aging test of VCSEL chips.

current control (ACC) drive, with sample sizes of 20 and 50 respectively.

Based on an assumption for both VCSEL and TOSA the life expectancy is reached at the point where opti-

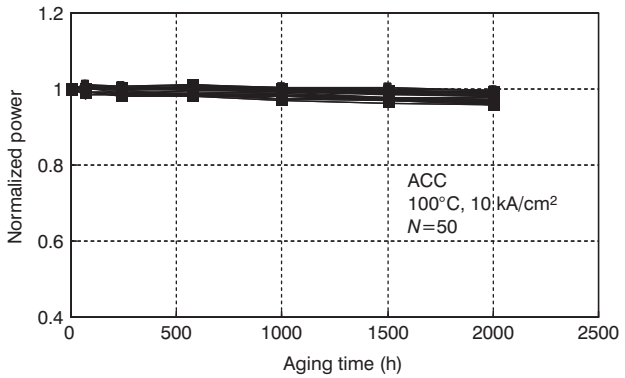

Figure 18 Results of aging test of TOSA.

cal power is reduced by 2 dB from the initial value, life expectancy was estimated to be approximately 50,000 hr at 100°C ambient. Converted to room temperature, this is equivalent to a life expectancy of 90 million hours (activation energy is 1.0 eV).

4. INTRODUCTION TO MASS PRODUCTION

Since, unlike ordinary edge-emitting lasers, VCSELs emit light in a direction perpendicular to the substrate, they have the characteristic that they can be tested at the wafer level. Here we will describe a burn-in test that, taking advantage of this characteristic, is carried out at the wafer level. Figure 19 is a photograph of a burn-in test being carried out at wafer level. Current was applied by probe directly to pad electrodes on the wafer. The wafer was heated by being placed on a heater table. Since ordinary burn-in tests are carried out after mounting on a TO-CAN, they involve enormous costs for test equipment and materials. In this method, by comparison, burn-in testing can be carried out for an entire wafer at once, thereby reducing the material cost when defects occur and providing an effective means for lowering the cost of mass production.

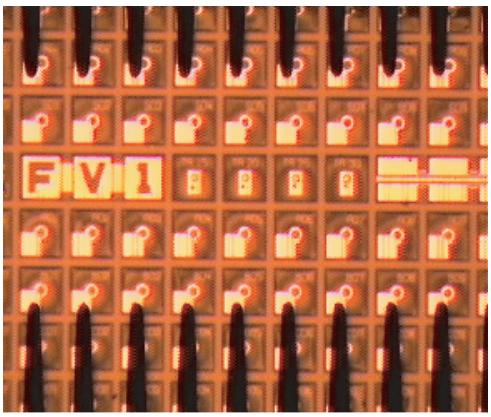

Figure 19 Example of burn-in test at wafer level.

5. CONCLUSION

We have a developed a 4.25-Gbps TOSA using 850-nm VCSEL for mounting in transceivers for data communications applications, for which a market take-off is anticipated.

Chip structure was optimized, after which its evaluation when mounted in the TOSA was carried out, and it was possible to achieve 4.25-Gbps operation, together with good results in terms of static characteristics and temperature characteristics that fully satisfied specifications. In reliability tests it was possible to obtain estimated life expectancies of 90 million hours at 25°C ambient and 50,000 hours at 100°C ambient.

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