Development of Wafer-Level Chip Size Package (WL-CSP)

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ABSTRACT Recently electronic equipment have remarkably improved becoming more compact and lighter and having upgraded function, requiring semiconductor packages mounted thereon to be more compact, thin-bodied and lightweight as well as to enable high-density mounting on substrates. Thus a new semiconductor package called wafer-level chip size package (hereafter called WL-CSP) technology is drawing attention. In response to such situations, the authors have developed a new WL-CSP, in which a tape substrate is bonded with wafers in a continuous roll-to-roll manufacturing process enabling cost reduction and quick delivery, and a resin post structure is adopted for the terminal pads to ensure high reliability. This paper reports on the structure, manufacturing process and results of prototype manufacturing of Furukawa Electric's original WL-CSP, together with its features and reliability test results.

1. INTRODUCTION

Recently electronics products represented by mobile phones, mobile computers, personal digital assistance (PDA) and digital still cameras (DSC) have been remarkably improved becoming more compact and lighter and having upgraded function. Along with such market trends, semiconductor packages mounted on these electronics products are keenly required to be more compact, thin-bodied and lightweight as well as to enable high-density mounting on substrates. See Figure 1.

Against this background, a new semiconductor packaging technology called WL-CSP is drawing attention, where

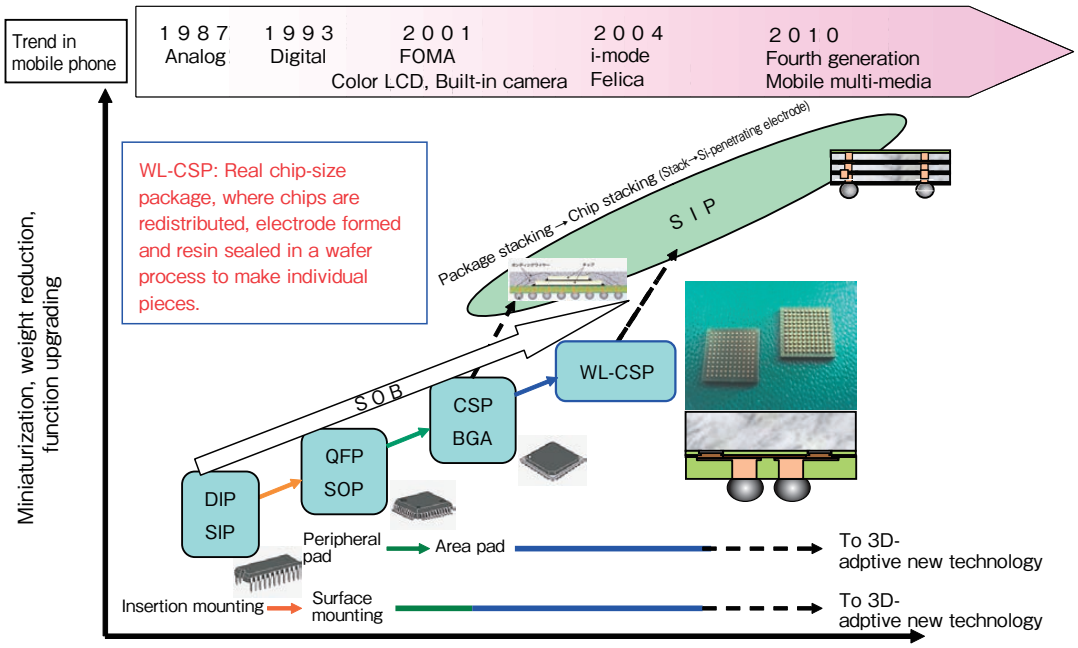

Figure 1 Trend in semiconductor packaging technology.

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chips are packaged plainly as in the wafer state. In the WL-CSP process, all the steps including redistribution, electrode formation, resin sealing and dicing are carried out in a series of wafer processes, and the size of a semiconductor chip finally cut from the wafer corresponds to its package size. Thus the WL-CSP process can be said ideal from the standpoint of miniaturization and weight reduction, so that the process has already been employed in mobile phones and so forth. We have developed a new WL-CSP manufacturing technology, in which a soldered tape substrate is bonded to wafers enabling quick delivery and cost reduction. And we have adopted a resin post structure for the terminal pads on the mounting substrate, and confirmed its high reliability. In this paper, the achievements of this high-bonding reliability WL-CSP manufactured by the new process will be reported.

2. DEVELOPMENTAL BACKGROUND OF FURUKAWA'S WL-CSP

Furukawa Electric has developed FBTI (Flexible Bumped Tape Interposer) [1] as an interposer for semiconductor devices to cope with weight reduction, height lessening and speed upgrading, and began marketing the product in 2001. The FBTI is an interposer designed on the presumption of using flip-chip bonding that is more suited for space saving and high-frequency operation than the conventional wire bonding. As shown in Figures 2 and 3, the interposer comprises SnAg solder bumps formed on a tape substrate to be used for electrical connection with semiconductor chips. The FBTI which may be called a tape substrate with soldered bumps is manufactured by a continuous method named roll-to-roll method, aiming at cost reduction.

The FBTI has been applied to semiconductor packages called TQON (Thin Quad Outline Non-Leaded) and SBM (System Block Module) at Toshiba Semiconductor Company. The structure of these products is such that Au stud bumps formed on semiconductor chips are flip-chip bonded to SnAg solder bumps on the FBTI, and high reliability has been confirmed in these applications. In view of these achievements, and based on the idea of combining the two technologies, i.e., the tape substrate manufacturing technology for FBTI aiming at cost reduction and the flip-chip bonding technology having proven reliability through applications, we considered it was highly feasible to realize Furukawa's original WL-CSP, and embarked on the development accordingly.

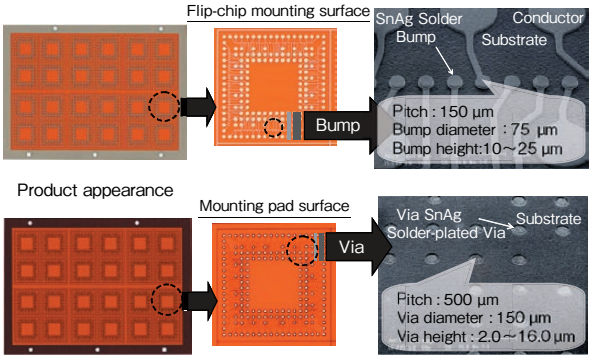

Figure 2 Appearance of FBTI.

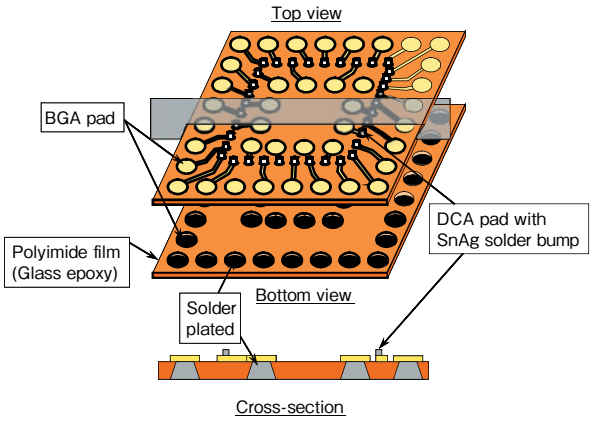

Figure 3 Schematic structure of FBTI.

3. CONCEPT OF FURUKAWA'S WL-CPS

Figures 4 and 5 show the structures of copper post-type WL-CSP with an established track record in the market and Furukawa's WL-CSP, respectively. The copper post-type WL-CSP commercially available has a characteristic structure in which copper posts 100 μm in height are formed on the wafer redistribution to ensure the reliability of mounting with the substrate. The manufacturing process of the copper post-type WL-CSP includes forming of redistribution to build routing circuitry on the wafer, formation of copper posts and resin sealing, necessitating special manufacturing equipment required by the wafer process. Moreover, the plating process for formation of copper posts constituting the characteristic structure takes much time, and the delivery time allegedly takes a rather long time because the manufacturing starts at the time of wafer reception.

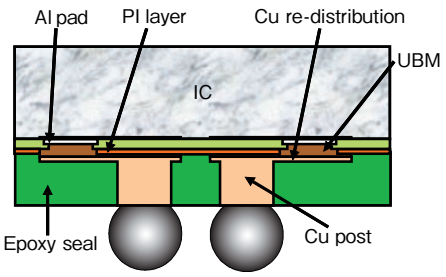

Figure 4 Schematic structure of commercially available WL-CSP.

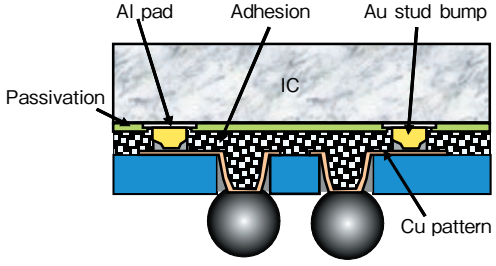

Figure 5 Schematic structure of Furukawa's WL-CSP.

On the other hand, the manufacturing process of the Furukawa's WL-CSP can be broadly divided into three: manufacturing of the tape substrate with resin posts, formation of Au stud bumps on the wafer and bonding of the wafer and the tape substrate. See Figure 6. With regard to the manufacturing process of the tape substrate with resin posts, application of the roll-to-roll manufacturing process for tape substrates with an established track record for FBTI is expected to result in cost reductions. Moreover, because manufacturing of the tape substrate can be started upon receipt of design information on the wafer, only the later manufacturing processes of Au stud bump formation and bonding of the wafer and the tape substrate are to be carried out after receipt of the wafer, thus enabling quick delivery.

The structure of Furukawa's WL-CSP is characterized by its terminal pad --called resin post, containing resin. WL-CSPs are generally used with their terminal pads loaded with solder balls, and they are mounted on the mounting substrate. The mounting reliability of electronic components such as semiconductor packages is usually evaluated by means of thermal shock test. In the case of WL-CSP which is mounted on substrates using solder balls, its reliability is influenced by a cracking mechanism such that a mechanical stress is applied to the solder balls due to the difference in the coefficients of thermal expansion between a semiconductor chip made of silicon and a mounting substrate called FR-4 printed circuit board, generating cracks either between the WL-CSP and the solder balls or between the mounting substrate and the solder balls. These cracks can grow to cause fatigue failures, and this constitutes a main cause of malfunction. That is to say, in terms of reliability test conditions, the lower the stress on the solder balls, the longer the lifetime until failure. Stress analysis based on simulation of the terminal pad structure shows, as illustrated in Figures 7 and 8, that the resin post structure results in a reduced maximum stress at the solder joints than the copper post structure, and thus it is expected that the joint lifetime is improved.

In the Furukawa's WL-CSP, moreover, the Au stud bumps on the wafer (i.e., semiconductor chip) are flip-chip bonded to the solder bumps on the tape substrate. Since this flip-chip bonding of Au to SnAg has a track record in semiconductor packages as mentioned before, and this structure is advantageous in terms of high-frequency operation, the Furukawa's WL-CSP is thought to be promising to cope with a high-speed memory device named DDR3-DRAM which will come on the market in the future.

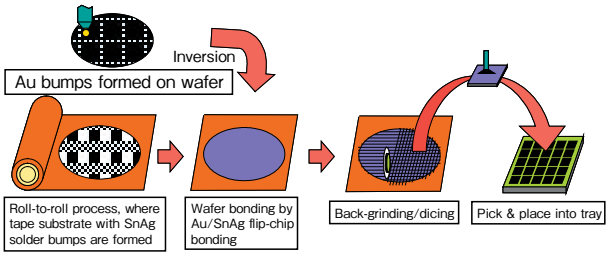

Figure 6 Concept of Furukawa's WL-CSP manufacturing process.

4. TECHNOLOGICAL PROBLEMS WITH FURUKAWA'S WL-CSP

In the manufacturing process of commercially available WL-CSP, routing circuitry is formed on the wafer, so that the wafer processes including direct application of photo-definable elastomer on the wafer, exposure, development, metal plating, and etching are carried out directly on the wafer. Wafer processes for semiconductors are typically employed to deal with the crucial points of manufacturing such as precise alignment of the exposure mask on to the wafer. On the other hand, manufacturing of Furukawa's WL-CSP comprises, differing completely from that of commercially available WL-CSP, the process of flip-chip bonding the Au stud bumps formed on the wafer to the solder bumps formed on the tape substrate, and this presented two major technological problems. One is the high level of dimensional accuracy required for the tape substrate, and the other is high-precision bonding of the tape substrate and the wafer.

The dimensional accuracy required for the tape substrate depends on the design parameters such as I/O pad pitch of the semiconductor chip, and can be derived as shown in Figure 9, which was calculated on the following assumptions; formation accuracy of Au stud bumps: ±3.5 μm; mounting accuracy between tape substrate and

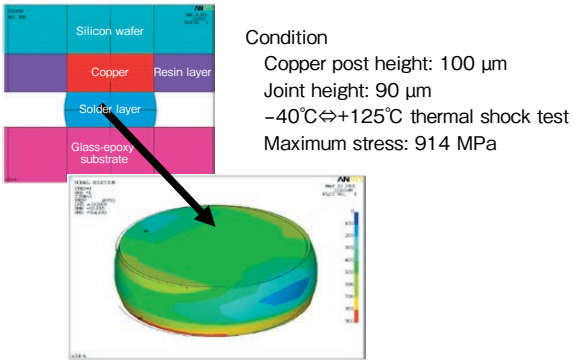

Figure 7 Calculated stress distribution of commercially available WL-CSP.

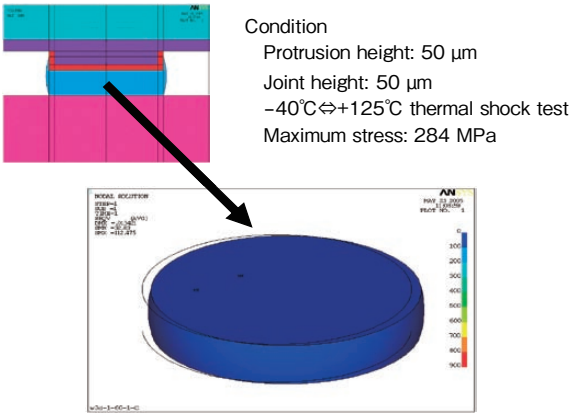

Figure 8 Calculated stress distribution of Furukawa's WL-CSP.

wafer: ±5 μm; tip diameter of Au stud bump: 15 μmϕ; and minimum gap: 25 μm. It can be seen that, assuming an I/O pad pitch of 80 μm for a semiconductor chip using 8-in wafer, the position accuracy of the solder bumps on the tape substrate is required to be not greater than about 19 μm over 100 mm (i.e., the center to periphery distance of 8-in wafer). In the future, if the I/O pad pitch of semiconductor chips becomes narrower, or larger wafers (say 12-in) are used, it would be necessary to take appropriate measures to cope with such changes, including: 1) to reduce the tip diameter of Au stud bump, 2) to adopt narrower minimum gaps, and 3) to improve the accuracy of tape substrate. In manufacturing the tape substrate for the Furukawa's WL-CSP, material handling of substrate and suppression of its deformation constitute important technical points because the continuous manufacturing scheme of roll-to-roll method is employed together with the use of tape substrates susceptible to deformation. By combining appropriate measures such as selection of fixing carrier material for the substrate, ingenious fixation method and circuit formation method, we have succeeded in achieving a position accuracy of ±5 μm. See Figure 10. To improve the position accuracy further, it would be necessary to control the tape manufacturing environment including temperature and humidity.

Bonding process of the tape substrate and wafer after alignment, constituting the second problem, is also specific to the Furukawa's WL-CSP. Mounting accuracy at this process obviously influences the position accuracy of the substrate, so that bonding equipment is required to be as good as possible in mounting accuracy. We investigated the market to acquire some equipment with a mounting accuracy specification of ±5 μm, but due to its unique process behaviors we were unable to find out any. Accordingly, we at the Production Technology Development Center developed an alignment press machine in-house, and the machine is currently used to manufacture prototype products for performance evaluation. See Figure 11. At present, when a tape substrate and wafer are bonded together, the position accuracy of Au stud bumps in relation to solder bumps has been confirmed to be satisfactory. See Figure 12.

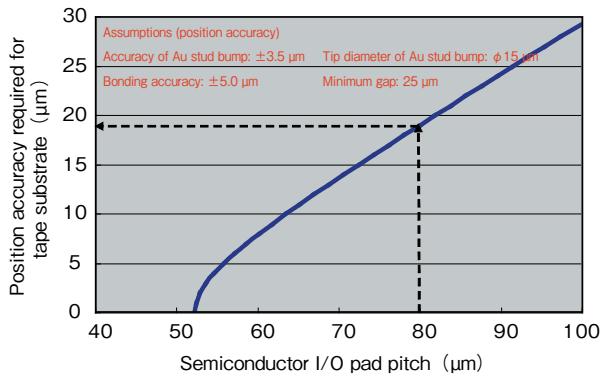

Figure 9 Position accuracy required for the tape substrate.

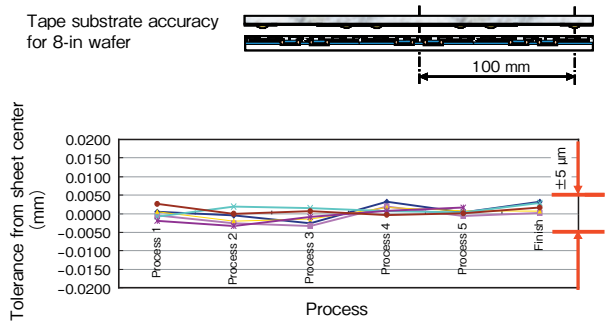

Figure 10 Position accuracy of solder bumps on the tape substrate.

5. RELIABILITY EVALUATION

Reliability evaluation procedures can be divided into reliability evaluation of the WL-CSP itself (hereafter called primary mounting reliability evaluation) and that of the substrate-mounted WL-CSP using solder balls (hereafter

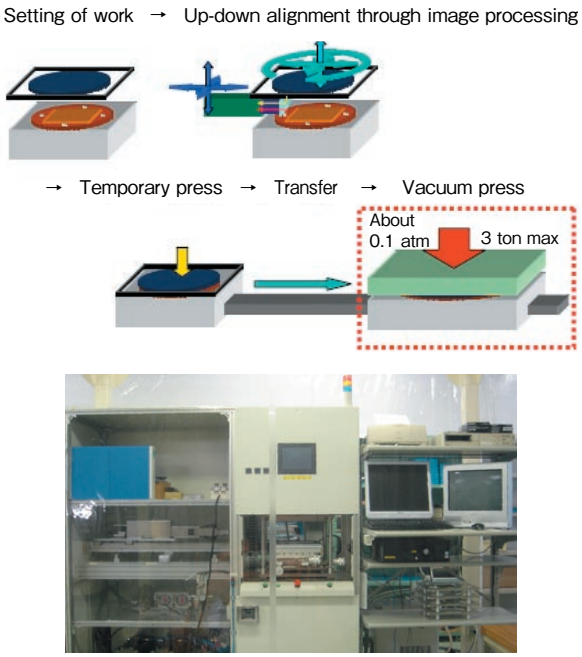

Figure 11 Appearance of alignment press machine.

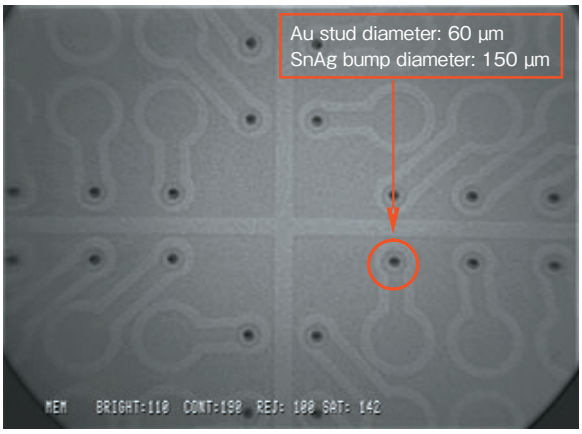

Figure 12 Confirmation of position accuracy of WL-CSP using soft X-ray image.

called secondary mounting reliability evaluation).

The sample chip used for reliability evaluation is an evaluation TEG chip 6.3-mm square having pads of 48 pins around the chip periphery, as shown in Figure 13.

5.1 Reliability of Primary Mounting

The tape substrate was designed in such a way that, when a WL-CSP consisting of a TEG chip and tape substrate is mounted on a substrate for secondary mounting reliability evaluation, a daisy chain is formed. Bonding conditions of the tape substrate to the wafer was optimized in terms of deformation of Au stud bumps, flow of SnAg solder around Au stud bumps, and thickness of the insulation layer.

With respect to the contents of evaluation, after each test item shown in Table 1 was performed, the terminal pads were confirmed for presence or absence of conduction by the four-terminal method, along with abnormalities confirmation by observation of the appearance and the cross-section. In the cross-section observation especially, close attention was paid to crack generation at the Au/SnAg bonding portions as well as to layer peeling at the semiconductor chip/adhesive layer and at the tape substrate/adhesive layer.

The results of reliability evaluation for the current prototyping show that all samples passed the tests satisfactorily as shown in Table 1, demonstrating excellent reliability of this semiconductor package. Thus reliability of Au/SnAg flip-chip bonding was confirmed.

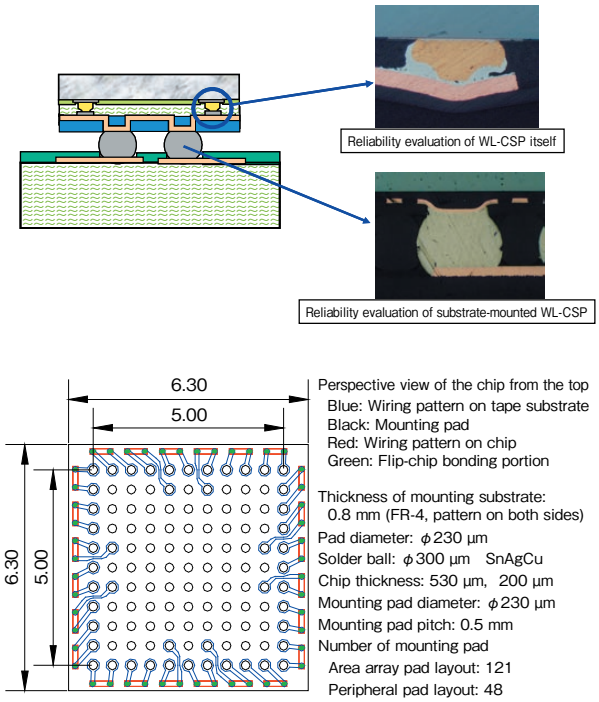

Figure 13 Sample for reliability evaluation.

Table 1 Conditions and results of PKG reliability test.

Test	Condition	Failure rate
Thermal shock	−65 ⇔ 150℃ 1,000 cycles	0/22
High temp. storage	150℃ 1,000 hrs	0/10
Autoclave	121℃ 85%RH 500 hrs	0/10
Pre-conditioning (JEDEC)	85℃ 85%RH 168 hrs 250℃ reflow 3 pass	0/22

5.2 Reliability of Secondary Mounting

The most commonly used printed circuit board of FR-4 was adopted as a substrate for evaluating the mounting reliability. The mounting pad pitch was 0.5 mm, and SnAgCu solder balls 0.3 mm in diameter were used. Two types of samples were evaluated paying attention to the chip thickness and solder ball layout, and the results are shown in Figure 14. One was in peripheral pad layout having 48 mounting solder balls on the periphery ---the minimum number necessary for creating a daisy chain, and its chip thickness was 530 µm, while the other was in an area array pad layout having solder balls at a 0.5-mm pitch, and its chip thickness was 200 µm.

Figure 15 is the Weibull distribution of the failure rates obtained by the reliability evaluation, where the conduction of the daisy chain created by the mounting substrate and WL-CSP was monitored during thermal shock test (−40℃ to 125℃, held 7 min at each temperature). The blue line shows the results for peripheral pad layout using solder balls with a chip thickness of 530 µm, whereby it is demonstrated that the initial development target of 400 cycles at a failure rate of 1% has been achieved. The red line in turn shows the results for area array pad layout using solder balls with a chip thickness of 200 µm, corresponding to a total package thickness of 280 µm excluding solder balls. It can be seen that better results are obtained here, rendering not only small area packages but also thin packages sufficiently promising. With commercially available WL-CSPs, it is allegedly difficult to

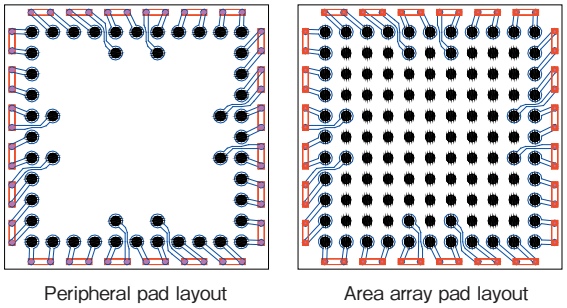

Figure 14 Comparison of surface mounting methods.

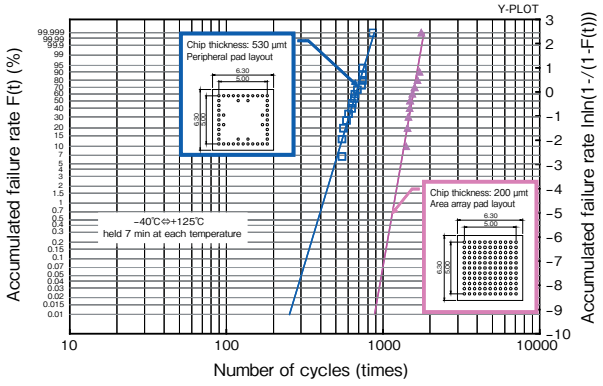

Figure 15 Solder joint reliability test results.

reduce the chip thickness due to rather large stresses resulting from the fact that the copper post is 100 μm in height and that a thick resin layer is used to embed the copper posts. In contrast with this, Furukawa's WL-CSP has great possibilities of reducing the chip thickness lower than that evaluated at this time, because it undergoes back grinding process after bonding the wafer and the tape substrate.

Now let us consider the failure mechanism of WL-CSP. Failure analysis of cross-sections observed after thermal shock tests suggests that failures occur between the solder ball and the mounting substrate or the WL-CSP, and more precise observation reveals that cracks are created at the interface between CuSn compound ---a hard substance made by diffusion of copper into solder, and solder which is rather soft. With respect to the location of fracture occurrence, a major influence is exerted on the solder balls on the four corners, because these are where the stress due to the difference in the coefficients of thermal expansion between the semiconductor chip and the substrate tends to concentrate on. In accordance with this, in actual evaluation, it has been confirmed that conductivity NGs occur at the solder balls on the four corners very often.

Observation of peeled surfaces on the solder balls reveals a continuous striped pattern which runs perpendicularly from the WL-CSP's corners to the center. See Figure 16. From these analyses, it can be seen that the failure mechanism is such that due to repeated strains generated by the difference in the coefficients of thermal expansion between the semiconductor chip and the mounting substrate, cracks are generated at the interface between the hard metal compound layer and the soft solder layer, and they grow to cause fatigue fracture. Given the fact that the Furukawa's original WL-CSP having a proprietary structure of resin post fractures in the same mode as for the common BGA components mounted on substrates using solder balls, it can be said that they share the same concept of reliability for mounting substrates. From this standpoint, we are making efforts to promote study to ensure reduced height and improved reliability.

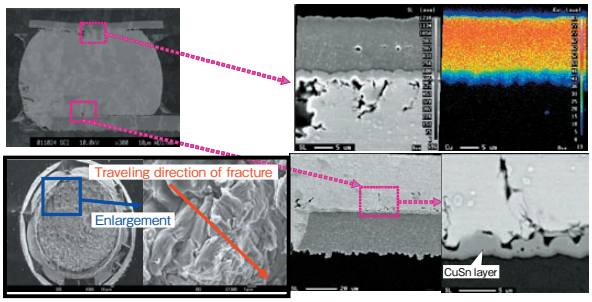

Figure 16 Analysis of failure.

6. CONCLUSION

We have recently developed WL-CSP, an ideal package in terms of miniaturization and weight reduction, using a manufacturing process completely different from conventional wafer process, whereby the tape substrate is bonded to the wafer. It has been confirmed that the new process makes quick delivery and reduced cost compatible, and bonding reliability for mounting substrates is ensured through the adoption of a new structure in which the terminal pads comprise resin posts. We have confirmed the possibility of thin-bodied packages using the WL-CSP, since good reliability has been confirmed for a thin package 200 μm in chip thickness, corresponding to a total package thickness of 280 μm excluding solder balls.

While commercially available WL-CSPs are only applied to high-yield wafers since they are manufactured by wafer processes, Furukawa's WL-CSP enables individual mounting of selected KGDs using a flip-chip bonder. Moreover, when it comes to semiconductor chips having multitudes of I/O pads, all the mounting pads can not be placed on the bottom face of the chip to configure the fan-in, but in case of individual mounting of chips the fan-out layout by placing mounting pads on the outside of the chip is permitted. Thus, this WL-CSP is expected to develop as a high-reliability semiconductor package with resin posts for terminal pads.

REFERENCE

1) Hikasa et al., "Development of Flexible Bumped Tape Interposer", Furukawa Review, No.24, pp.59-64 (2003)