High-Power GaN HFETs on Si Substrate

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ABSTRACT Epitaxial growth technology for GaN devices on large-diameter Si substrate has been studied in this paper, which is essential for device cost reduction. In an effort to improve the buffer breakdown voltage for increasing the breakdown voltage of the device, carbon concentration in the GaN layer is controlled to find that the carbon concentration significantly contributed to buffer breakdown voltage improvements. Device performance is evaluated for the devices with an AlGaN/GaN HFET structure on Si substrate, and it is shown that the performance was equivalent to that of the device on sapphire substrate. A large-area device having this structure is fabricated in order to confirm its potential as a power device, and a current capacity of 120 A or more and a breakdown voltage of 1.3 kV has been achieved. On the other hand, with respect to the problematical issue of current collapse in GaN HFETs, the HFET structure on Si substrate has resulted in a significant improvement compared with the structure on sapphire substrate, thus realizing a high-performance device that does not show a salient current collapse up to 900 V.

1. INTRODUCTION

The device development of GaN, a wide bandgap semiconductor like SiC, is proceeding in expectation of characteristics superior to those of conventional Si-based semiconductors. In particular, GaN-based field effect transistors (FETs) are able to operate at high power, high frequencies and high temperatures, exhibiting various excellent performance indexes [1)~3)]. In contrast to conventional Si devices, those based on wide bandgap semiconductors such as SiC and GaN offer significantly better performance overcoming the so-called "silicon limit", so that it is expected that they can realize high-performance power supplies in terms of low power loss, compactness and high efficiency, which was unachievable with conventional Si devices.

With respect to epitaxial growth of GaN, recent advancement in crystal growth technology has made it possible to use Si for the substrate, thereby achieving crystal growth of thick epitaxial layers on large diameter Si wafers, which has been difficult conventionally. Introducing an MOCVD (Metal Organic Chemical Vapor Deposition) machine capable of multi-wafer crystal growth using 4-in Si wafers, we have been investigating the crystal growth technology. In this paper, experimental results of GaN epitaxial layer growth on a 4-in Si wafer for high-breakdown voltage devices will be presented.

Fabrication of relatively large-area devices is needed to demonstrate the potential of a power device in general. In the case of HFETs on Si substrate, however, in contrast to in the case of sapphire substrate, it is essential to reduce the leak current in the buffer layer so as to realize a device with a high breakdown voltage, and this requires some inventive processing techniques. With regard to current enhancement, we have applied our unique structure to the electrode, thereby achieving good large-current performance [6)]. In terms of breakdown voltage performance, thick epitaxial layers of high resistance based on carbon doping were used, and, simultaneously, a deep mesa structure was formed by dry etching to achieve high output power.

On the other hand, the AlGaN/GaN HFET offers a high-output, high-switching-speed device taking advantage of its high-mobility, high-density, two-dimensional electron gas layer formed on the interface, and the device is under development. However, suppression of current collapse is essential for practical use of GaN HFETs. Several research institutes have so far reported on the effects of application of a field plate (FP) structure and so on to suppress the current collapse [4), 5)]. In this paper, current collapse has been evaluated for the HFETs with different substrates and structures.

2. RESULTS AND DISCUSSION

2.1 Results of Epitaxial Layer Growth on 4-in Si Wafer

In the past, we used 2-in Si (111) wafer for epitaxial growth, whereby a GaN/AlGaN HFET structure was formed on a buffer layer to obtain breakdown voltages in

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excess of 400 V [7]. But since use of large-sized wafers is indispensable for reducing the device cost, we have recently introduced an MOCVD machine capable of processing five 4-in wafers at a time, and have since been investigating epitaxial growth using 4-in Si (111) wafer and TMGa, TMA1, and NH_3 gases [8].

Figure 1 shows the AFM observation result of a surface after growth. It is seen that a crack-free smooth surface is obtained in spite of the use of 4-in Si wafer. The surface has an RMS roughness of 0.54 nm, and terraces due to atomic step can be observed. Figure 2 shows the results of thickness distribution evaluation for GaN epitaxial layer on 4-in Si wafer, in which evaluation is done in two directions, vertical and horizontal, with respect to orientation flat (OF). The index of distribution is calculated, by dividing the standard deviation by the average, to be 2.9%. Figure 3 shows a comparison of GaN layer thickness between 4-in Si wafers. Excellent wafer-to-wafer distribution is obtained with a distribution index of 0.5 % or lower. As mentioned above, it may be concluded that the epitaxial growth conditions developed here have characteristics sufficient to realize high throughput.

It is thought that there are two crucial factors in improving the breakdown voltage of the device. One is enhancement of the resistance of epitaxial layers including the buffer layer, and the other is increasing the thickness of epitaxial layers. Whereas the breakdown voltage for buffer layers conventionally obtained using the 2-in machine was 500 V or higher, the same layer structure formed on a 4-in wafer was found to result in a problematic value of approximately 200 V. We investigated the cause of the breakdown voltage decrease, and it was suggested that a leak current was generated due to the existence of carriers caused possibly by nitrogen vacancies, which resulted in the degradation in breakdown voltage. Accordingly we tried to compensate for the nitrogen vacancies by proactively using a dopant. Carbon, one of the candidate dopants, is expected to show a small coefficient of diffusion in GaN, so that, if suitable growth conditions are selected, it can be used as a dopant provided with superior diffusion controllability in the depth direction. Figure 4 shows the schematic of a sample device for breakdown voltage measurement of the buffer layer. In the experiment, by changing the growth conditions, GaN layers with different carbon concentrations were grown on the buffer layer, on which a high-concentration n-GaN layer was grown to form an ohmic contact. A device for breakdown voltage measurement was formed by etching the n-GaN layer between the electrodes. Figure 5 shows the breakdown voltage of buffer layer versus carbon concentration in the i-GaN layer estimated by SIMS. The distance between the electrodes was kept at 10 μm to facilitate comparison. Auto-doping of carbon was carried out by

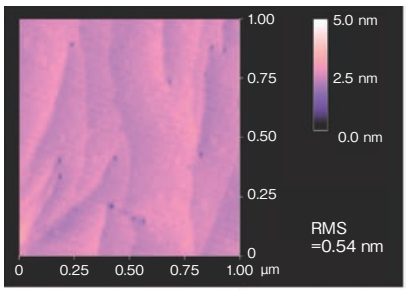

Figure 1 AFM image of GaN epitaxial layer on a 4-in Si wafer.

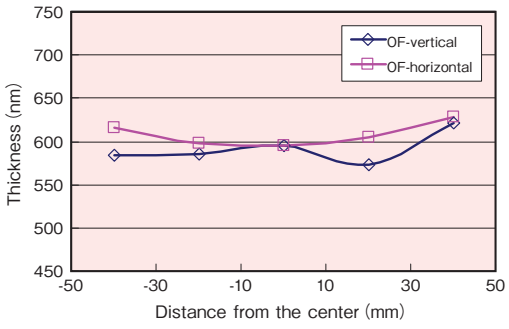

Figure 2 Thickness distributions of GaN layers on a 4-in Si wafer.

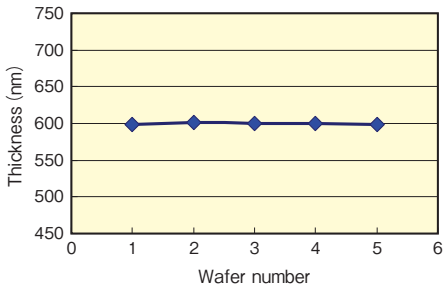

Figure 3 Comparison of GaN layer thickness among 4-in Si wafers.

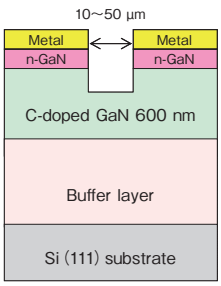

Figure 4 Schematic of GaN-based epitaxial layer sample for breakdown voltage measurement.

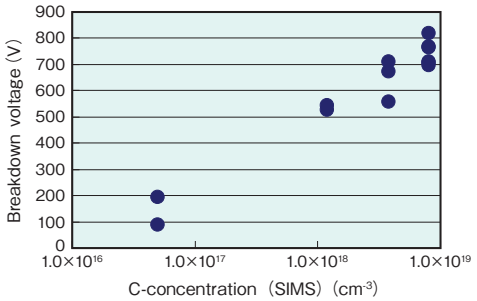

Figure 5 Breakdown voltage versus carbon concentration.

controlling the growth conditions. It can be seen that the carbon concentration is controlled from 10^{16} cm^{-3} to near 10^{19} cm^{-3}, and that the breakdown voltage increases depending on the carbon concentration. As the result, it has been shown that breakdown voltages in excess of 800 V can be obtained.

In order to increase the total thickness of epitaxial layers, on the other hand, it is required to devise suitable growth conditions and structures so that epitaxial layers with minimized crack and warpage can be obtained. We have optimized the conditions based on AlN/GaN structure, thereby succeeding in realizing a maximum total thickness of 5.2 μm. Figure 6 shows the evaluation results of breakdown voltage versus electrode distance. As can be seen, in the case of total epitaxial layer thickness of 2.3 μm, the breakdown voltage increases as the electrode distance increases up to 20 μm, achieving a maximum value of 800 V. Above 20 μm, however, the breakdown voltage remains unchanged showing a tendency to saturate. In the case of 5.2-μm thick epitaxial layers, the breakdown voltage also increases with increasing electrode distance, reaching 1,700 V or higher at an electrode distance of 30 μm, above which a tendency to saturate can be seen. To summarize, we may conclude that the breakdown voltage of epitaxial layers improves with increasing layer thickness. Figure 7 plots the maximum breakdown voltage for various layer thicknesses, showing that the maximum breakdown voltage improves virtually in a linear relationship as the total thickness of epitaxial layers increases. Thus it was decided to proceed to device fabrication and characteristics evaluation based on the investigation results mentioned above.

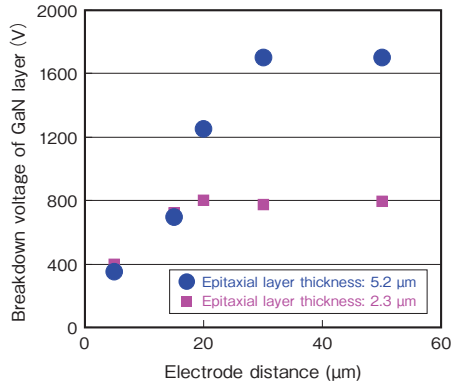

Figure 6 Dependence of breakdown voltage on electrode distance for different total epitaxial thicknesses.

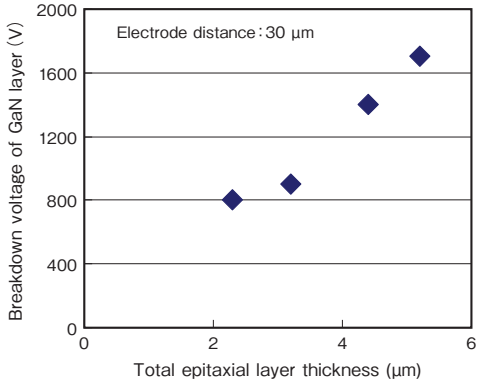

Figure 7 Dependence of breakdown voltage on total epitaxial layer thickness.

2.2 Evaluation Results of Device Characteristics

Epitaxial layers of AlGaN/GaN HFET structure were fabricated on a Si (111) substrate by means of MOCVD, and comparisons were made with those formed on a C-face sapphire substrate. Prototyping of devices was carried out using chlorine-based ICP (Inductively Coupled Plasma) equipment to form mesa structure, the sputtering method to form electrodes, and the PCVD (Plasma Chemical Vapor Deposition) method to deposit SiO_2 as a passivation layer and an inter-layer insulation layer. Figure 8 shows the photograph of a 4-in Si wafer with GaN epitaxial layers after processing of mesa etching and electrode forming. Since the wafer shows less significant warpage making the epitaxial layers suitable for post-processing, it is possible to process the 4-in wafer intact in a circular shape. Figure 9 shows the device structure formed on Si wafer prototyped here, in which a deep mesa is formed to reach the Si substrate to improve the breakdown voltage, and the fingers are plated to reduce the electrode resistance.

Devices were fabricated using epitaxial layers with different thicknesses. Figure 10 shows the DC characteris-

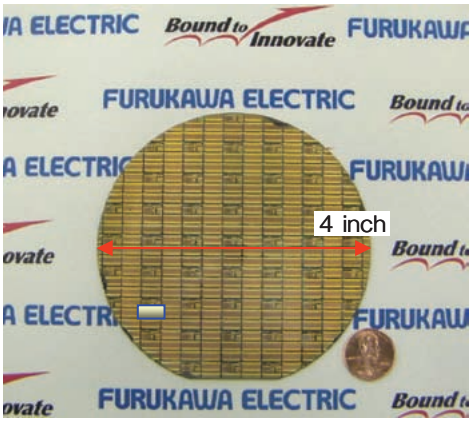

Figure 8 Photograph of post-processed 4-in wafer.

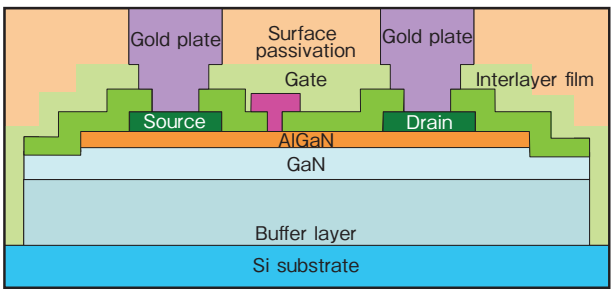

Figure 9 Schematic of HFET device structure on Si substrate.

tics of the devices. Figure 10 (a) shows the results for the device on sapphire substrate and Figure 10 (b) on Si substrate. The parameters for the devices evaluated here are as follows: total thickness of epitaxial layers on Si substrate is 3.5 μm; sheet resistance for the both substrates is about 500 Ω/□; gate width W_g = 200 μm; gate length L_g = 2 μm; and gate-to-drain distance L_{gd} = 10 μm. In the case of the device on Si substrate, it was shown that the current at a gate-to-source voltage V_{gs} = 1V was 350 mA/mm or more, and the on-resistance was 10.4 Ωmm, a satisfactory value. In the case of the device on sapphire substrate, comparable results were obtained for the current and on-resistance. Meanwhile, Figure 11 shows the results for the 5.2-μm epitaxial layers on Si substrate with L_{gd} = 15 μm. The on-resistance is somewhat larger--13.4 Ωmm, which may be attributed to the fact that the sheet resistance--630 Ω/□--is somewhat higher than that of the epitaxial layers in Figure 10.

The devices with different L_{gd} values fabricated on Si substrate were evaluated for their gate-drain breakdown voltage. The evaluation was carried out using Flourinert to prevent creeping discharge, and with the electric potential of the substrate floating. Figure 12 shows the results for 5.2-μm thick epitaxial layers. The breakdown voltage increases as L_{gd} increases from 5 μm through 10 μm to 15 μm, reaching 1,500 V or higher at 15 μm. But at L_{gd} = 20 μm the breakdown voltage showed a tendency to saturate at 1,630 V. Since the breakdown voltage of the buffer layer of these epitaxial layers was around 1,700 V, it was shown that the gate-drain breakdown voltage was limited by the breakdown voltage of the buffer layer.

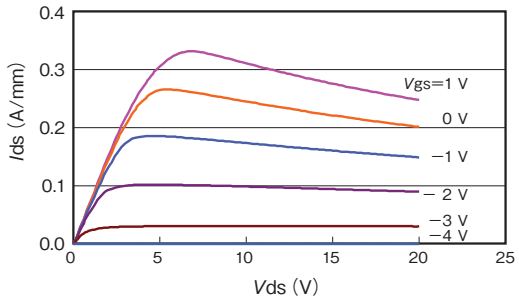

Figure 10 (a) DC characteristics of AlGaN/GaN HFET on sapphire substrate.

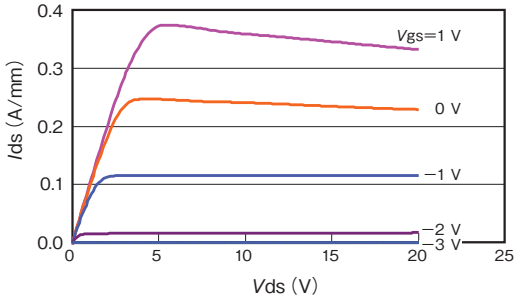

Figure 10 (b) DC characteristics of AlGaN/GaN HFET on Si substrate.

Figure 13 plots the gate-drain breakdown voltage with respect to L_{gd}, of devices with different epitaxial layer thicknesses. Whereas the breakdown voltage shows a tendency to saturate at about 1,100 V in the case of epitaxial layer thickness of 3.5 μm, in the case of the 5.2-μm thickness, the voltage tends to saturate above L_{gd} = 15 μm reaching 1,500 V or higher. And, in both cases, it is seen that the relationship is close to a linear line of

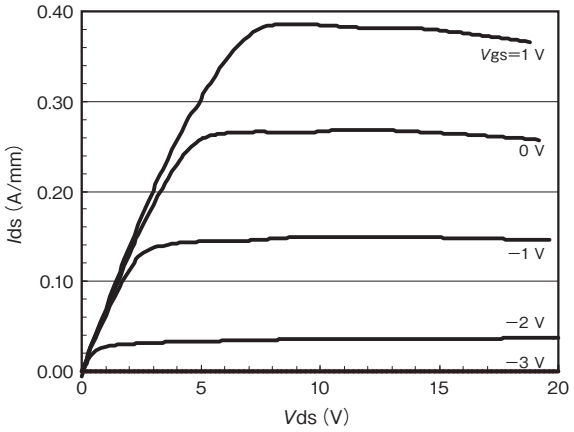

Figure 11 DC characteristics of HFET using 5.2-μm epitaxial layer on Si substrate.

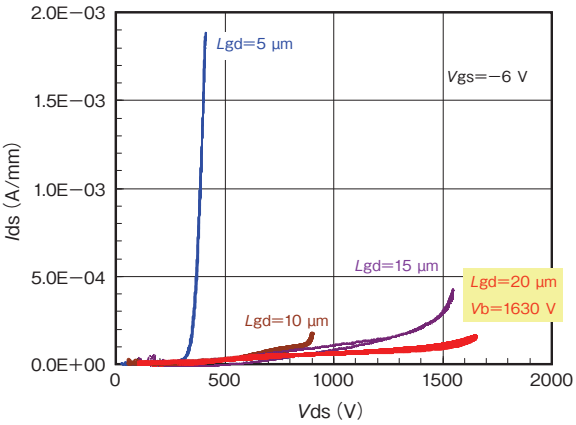

Figure 12 L_{gd} dependence of off-state characteristics for HFETs using 5.2-μm epitaxial layer.

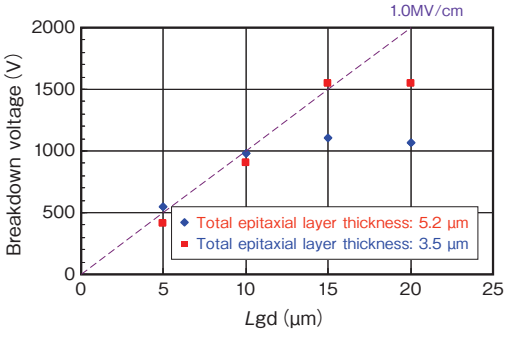

Figure 13 Breakdown voltage versus L_{gd} for small-area device HFETs with different total epitaxial layer thicknesses.

approximately 1.0 MV/cm, up to L_{gd} = 10 μm.

Next the results of formation of large-area devices will be presented. Figure 14 shows the photo of a large-area device fabricated here. Fingers are formed near the center, and pads for wire bonding are formed above and below. The size of finger area is 6.8 mm×1.5 mm.

The device mentioned above was evaluated for electrical characteristics. Figure 15 shows the measurement results of gate-drain breakdown voltage, in which a device with W_g = 340 mm and L_{gd} = 15 μm was evaluated. The measurement was carried out as on-wafer, so that a Fluorinert† immersion environment was used to prevent creeping discharge. A breakdown voltage of 1.3 kV was obtained at V_{gs} = −6 V. This result is recognized as the largest-ever value among the characteristics of high-power GaN HFETs on Si substrate ever achieved.

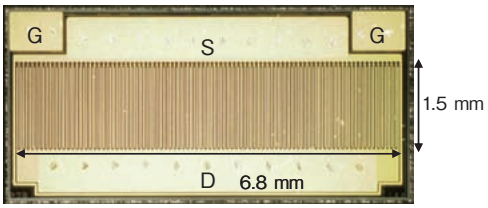

Figure 14 Photograph of HFET large-area device. (W_g = 340 mm)

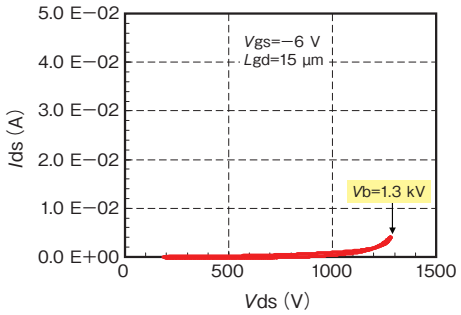

Figure 15 Off-state characteristics for large-area device. (W_g = 340 mm)

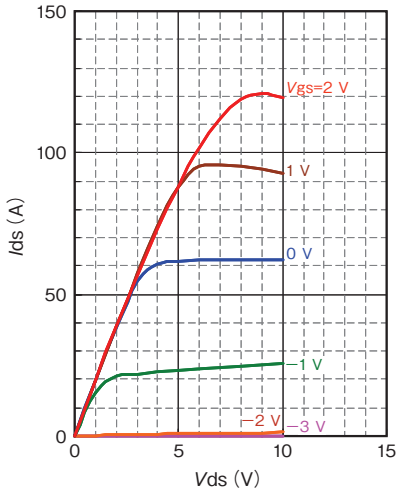

Figure 16 On-state characteristics for large-area device (W_g = 340 mm)

The device was mounted in a TO-220 package to be evaluated for the current-voltage characteristics. Figure 16 shows the results of drain current-voltage characteristics measurement for a device with W_g = 340 mm and L_{gd} = 15 μm, with changing V_{gs} from 2 V to -3 V. From the Figure superior current-voltage characteristics can be seen, and the maximum current of 120 A was obtained at V_{gs} = 2 V. Meanwhile, the on-resistance was 51 mΩ (5.2 mΩcm^2 when normalized by area).

2.3 Evaluation Results of Current Collapse Characteristics

Having demonstrated the device with a sufficient breakdown voltage, we moved to evaluate current collapse characteristics. For evaluation of current collapse, the so-called "pulse collapse method" has been used [4]. Although this method allows for on-wafer evaluation, it is somewhat complicated in that the matching resistance has to be changed to suit the device size, and so on. In order to establish a convenient measurement method for current collapse characteristics, we studied measurement methodology. Figure 17 illustrates the technique employed, in which the current collapse quantity is defined as the value of R_{on_af}/R_{on_bf}, where measurement is made to obtain initial on-resistance R_{on_bf}, off-state, and on-resistance R_{on_af}, in this order. First, both the on-wafer measurement and pulse collapse measurement methods were applied to the same device, and measurement conditions were optimized in order to obtain good correlation with the pulse collapse method. Since the conditions are strongly influenced by off-stress time $T_{\_off}$, experiments were carried out with various off-stress times, and as a result, it was found that $T_{\_off}$ = 10 sec resulted in best agreement with the pulse collapse method. Figure 18 shows the correlation between the two methods, in which measurement was made with $T_{\_off}$ = 10 sec. It can be seen that the pulse collapse method on the longitudinal axis has a linear relationship with respect to the on-wafer method on the lateral axis. From the above results we may say that a good correlation is established with the pulse collapse method, so that it has been decided to use hereafter this condition as an on-wafer current collapse evaluation technique.

Figure 19 shows the evaluation results of current col-

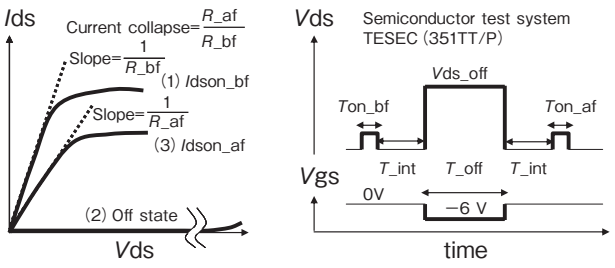

Figure 17 On-wafer evaluation method for current collapse characteristics.

† Fluorinert is a trademark of 3M.

lapse characteristics for various devices, in which the gate-drain electric field V_{ds_off} is plotted on the lateral axis and the current collapse quantity on the longitudinal axis. The measurements were made, on the devices with L_{gd} = 15 μm, on wafer, in a Fluorinert environment to prevent creeping discharge, and the substrate had equal potential with the source. The results for three epitaxial layers with different thickness on Si substrates are compared in the Figure, and the results for the devices on sapphire are shown for comparison. In the case of sapphire substrate, the current collapse is seen to increase as the drain voltage V_{ds_off} increases, reaching five times or higher at 400 V. In the case of the devices on Si substrate, on the other hand, the current collapse remains at a very low level even at high voltages, showing good results. This may be attributed to the fact that crystal quality of epitaxial layers on Si substrate has been much improved, and that electric field concentration has been relaxed by the field plate effect of Si substrate due to its conductivity. The marks ■, ●, and ■ in the Figure represent total epitaxial layer thicknesses of 2.5 μm, 3.4 μm, and 5.2 μm, respectively. In the case of the total epitaxial layer thickness of 2.5 μm, the current collapse quantity shows a relatively small change of 1.1 times up to 350 V, and subsequently breaking down at 400 V. In the case of 3.4 μm, it stayed constant at about 1.3 times up to 700 V, followed by a breakdown at 750 V. In the case of 5.2 μm, it remained at about 1.6 times up to 900 V, followed by a breakdown at 950 V. These results suggest that although breakdown voltage rises with increasing epitaxial layer thickness, current collapse also increases. If current collapse increases with increasing layer thickness as has been suggested, it is thought, some improvements must be made in order to resolve the tradeoff between epitaxial layer thickening for breakdown voltage enhancement and current collapse improvement. Here, field plate (FP) structure is generally considered as a measure for improving current collapse. Figure 20 shows its schematic. When a device has no FP structure, the electric field tends to concentrate on the drain-side end of the gate electrode. When the FP structure is employed, it comes in a structure such that the gate electrode is elongated to the drain side (i.e., G-FP), or the source electrode is extended to the drain side overlapping the gate electrode via an insulation layer (i.e., S-FP) [4]. We have investigated here whether application of FP structure improves current collapse characteristics.

Figure 21 shows the evaluation results of current collapse for the devices in the same lot using a 5.2-μm epitaxial layer, having different structures in terms of the gate-field plate length (L_{gfp}) and source-field plate length (L_{sfp}). It can be seen that the devices employing the FP structure has been improved in comparison to the devic-

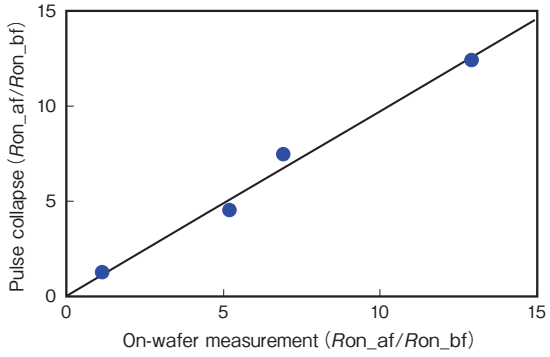

Figure 18 Correlation between pulse-collapse method and on-wafer method for current collapse characteristics.

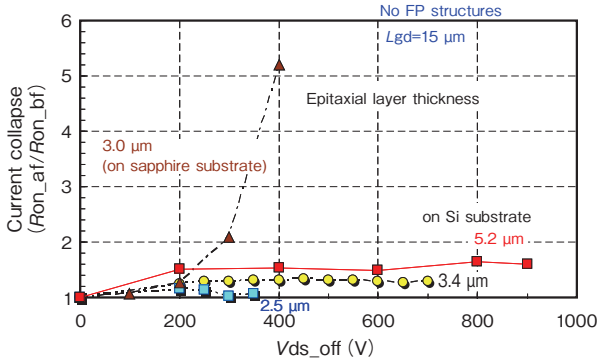

Figure 19 Dependence of current collapse characteristics on epitaxial layer thickness for different kinds of substrates.

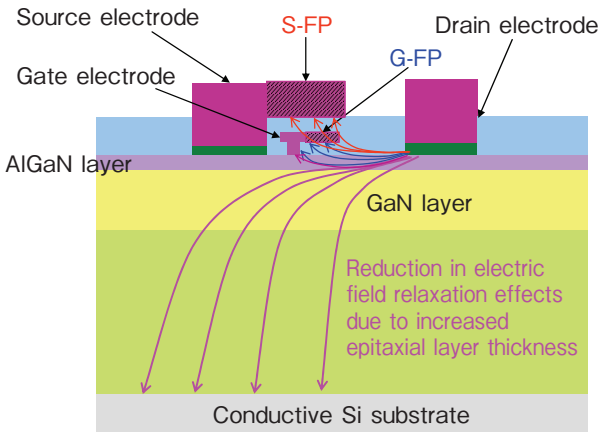

Figure 20 Suppression of current collapse using field plate structure.

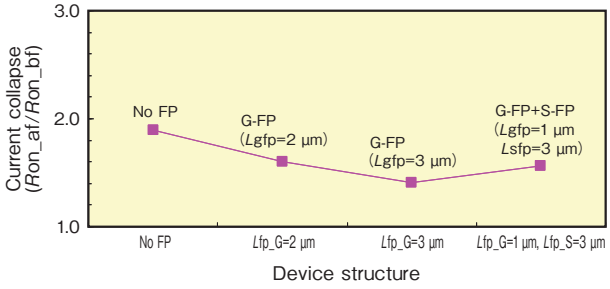

Figure 21 Comparison of current collapse between devices with and without field plate structures.

es without the FP structure, and that, in the case of G-FP structure, the current collapse improvement is dependent on the length. From the results mentioned above, it has been shown that the use of the FP structure suppresses the degradation of current collapse characteristics due to increased thickness in epitaxial layers.

CONCLUSION

Epitaxial growth technology for GaN layer on Si substrate has been studied aiming at a new device with high breakdown voltage and low on-resistance. Epitaxial layer growth using a 4-in multi-wafer machine is confirmed to result in good uniformity both in-wafer and wafer-to-wafer characteristics. In order to improve breakdown voltage performance, the carbon concentration in GaN layer is controlled as a technique to enhance the breakdown voltage of the buffer layer, and it has been found that the carbon concentration significantly contributes to breakdown voltage improvements. As the result, the maximum breakdown voltage of 1.7 kV has been obtained using a total epitaxial layer thickness of 5.2 μm.

The HFET structure is formed on the above mentioned epitaxial wafer to fabricate a device, and, as the result, a device having good characteristics of 1.3 kV in breakdown voltage, 120 A in maximum current, and 5.2 mΩcm^2 in on-resistance is obtained at W_g = 340 mm. The current collapse is evaluated, and it has been found that the current collapse can be suppressed low up to 900 V. Moreover, application of the FP structures has been studied to find out that current collapse can be suppressed further even in thick epitaxial wafers.

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