High-Power Operation of Normally-Off GaN MOSFETs

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ABSTRACT A power transistor to be incorporated into the power supply circuitry for automobiles and home appliances has been developed. The semiconductor material used is GaN that is characterized by its higher critical electric field and higher maximum saturation velocity than those of Si. A metal-oxide-semiconductor (MOS) structure of metal/SiO_2/GaN has been used to achieve normally-off operation in which no current flows unless a gate voltage is applied, since this operation is generally required for power transistors to ensure system safety. High-temperature, high-power operation of GaN MOSFETs has been realized here by improving the quality of the SiO_2/GaN interface thus reducing the contact resistance between the metal and GaN. The threshold voltage, breakdown voltage, operation current and maximum operation temperature were +3 V, higher than 1550 V, larger than 2.2 A and 250°C, respectively.

1. INTRODUCTION

Power transistors are incorporated as a switching element in power supply circuits like inverters. Since inverters can control motors by converting the frequency of AC power supply, they are widely used for energy-efficient motor control; and hence in hybrid cars, as well as in energy-saving home appliances such as air-conditioners and induction heating (IH)-based cooking devices and industrial motors. For this reason, great expectations are placed on the performance enhancement of power transistors, since this would result in loss reduction in inverters, achieving higher energy efficiency and leading to a contribution to environmental improvements.

Currently, Si-based insulated gate bipolar transistors (IGBTs) are used as power transistors. But their performance deteriorates drastically at high temperatures with a reduced operation current above 200°C [1]. This is largely attributable to the material performance of Si, so that it is absolutely imperative to develop a power transistor in near future using a new material, in order to realize a large output power and small on-resistance at high-temperature environments.

We recognized the potential of gallium nitride (GaN), a kind of nitride semiconductor, as a new material. GaN has a higher breakdown voltage and a higher saturation velocity than those of Si, and therefore, a GaN-based power transistor shows possibilities to realize a high breakdown voltage and low on-resistance [2), 3)]. Since reduction in the on-resistance means reduction in heat generation, this can also result in simplification of cooling systems such as heat sinks, thereby making a significant contribution to efficiency enhancement and downsizing of power supply circuits.

The structure of power transistors using GaN comes in two kinds: heterostructure field-effect transistor (HFET) and metal/oxide/semiconductor field-effect transistor (MOSFET). Until now, much work has been done on AlGaN/GaN-based HFETs. The reason is that a two-dimensional electron gas (2DEG) is generated at the AlGaN/GaN interface as a result of spontaneous and piezo polarization, making it possible to obtain high electron concentrations. However, AlGaN/GaN HFETs intrinsically show a negative threshold voltage, resulting in normally-on operation. Thus they need a drive circuit to control the gate bias, which leads to the necessity of additional study to cope with circuit complexity and cost increases. Especially in view of power device applications, the normally-off type transistor in which no current flows at no gate bias is strongly required from the application system side, and this requirement is justified when one considers any replacement of Si power transistors presently in use or the importance of malfunction prevention against possible surge voltages during power outages.

On the other hand, the MOSFET has the advantages of low gate leakage current and simple structures, in addition to the fact that its structure allows normally-off operation. Accordingly, a number of research institutions recently report on the performance of GaN MOSFETs [9)~13)]. Chow et al. have fabricated a GaN MOSFET that has achieved a threshold current of 3.3 V and operation current of 10 mA at 150°C [10)], but the current and temperature would require further improvements.

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Figure 1 shows developmental issues necessary for performance enhancement of GaN MOSFETs. Since the GaN crystal is usually prepared through heteroepitaxial growth on a substrate having a different lattice constant, the crystal contains a number of dislocations that affect device characteristics and reliability, so that it becomes essential to improve the crystalline quality. It is reported that a high crystalline quality of GaN can be obtained by inserting a buffer layer between the substrate and GaN crystal and by optimizing the growth conditions of the GaN crystal [14].

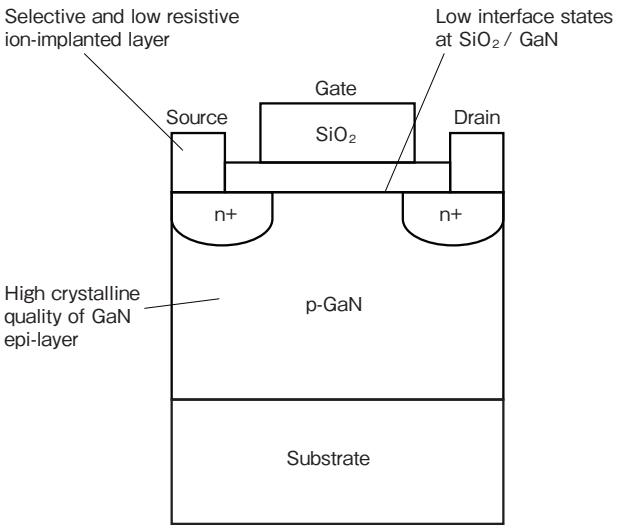

Figure 1 Developmental issues for performance enhancement of GaN MOSFETs.

What deserves special attention in the development tasks for the MOSFET here is, as shown in Figure 1, the quality improvement of the SiO_2/GaN interface and the resistance reduction for the contact layer selectively formed under the electrodes. In MOSFETs, a channel is formed on the GaN surface under the gate in which a current flows between the source and the drain thus effecting device operation. If the SiO_2/GaN interface has poor quality, electrons in the channel are captured at the interface states, so that the channel resistance increases. The threshold voltage also deviates from the design value, thereby posing the problem of ringing at switching. Therefore, it is essential to improve the quality of the SiO_2/GaN interface, or in other words, to reduce the interface states. With respect to the contact layer needed for current conduction between the metal and semiconductor, an n-type dopant of Si ion is implanted into p-type GaN crystal to selectively form an n-type conduction layer. It also becomes important to choose optimized implantation conditions to recover the damages generated due to implantation, as well as to find out optimum annealing conditions for activation of Si, in order to form a low-resistance contact layer.

In this report, the developmental history of ion implantation technologies aimed at quality enhancement of SiO_2/GaN interface and formation of low-resistance contact layer will be described first. Then, the device characteristics of GaN normally-off MOSFETs fabricated using these elemental technologies will be presented.

2. IMPROVEMENT OF SiO_2/GaN INTERFACE QUALITY [15), 16)]

MOS capacitor samples for evaluating the interface state density were fabricated, in which n-type GaN was used in order to investigate the near-bottom energy of conduction band. First, n-type GaN ($Nd^+ - Na^- \sim 2\times10^{17}$ cm^{-3}) 1 μm in thickness was grown on a sapphire substrate (0001)c by metal-organic chemical vapor deposition (MOCVD). The GaN surface was cleansed using common RCA cleaning, and SiO_2 50 nm in thickness was deposited by plasma-enhanced chemical vapor deposition (PECVD). After that, the sample was annealed in a nitrogen flow in an electric furnace, and subsequently, the ohmic electrode (Ti/AlSi/Mo) and gate electrode (Ti/Au) were formed by sputtering and lift-off process. Lastly, the capacitance-voltage (C-V) characteristics at 200°C were measured by an impedance analyzer, and the interface state density was calculated by the Terman method [17].

Figure 2 shows the interface state density distribution of the SiO_2/GaN-based MOS capacitor annealed at different temperatures. The interface state density is seen to decrease at higher annealing temperatures. In the case of 900°C, it is lower than 1×10^{11} cm^{-2}eV^{-1} at an energy position 0.4 V apart from the near-bottom energy of conduction band. These values are sufficiently low for satisfactory operation of the MOSFET device.

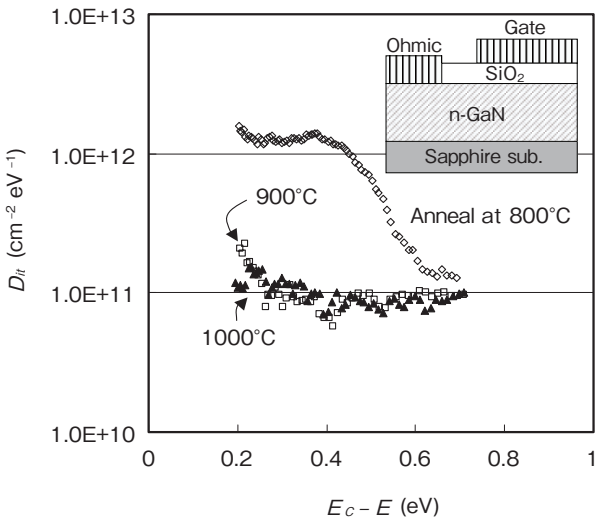

Figure 2 Interface state density (D_{it}) of SiO_2/GaN, annealed at 800, 900 and 1000°C.

3. Si ION IMPLANTATION IN GaN AND ITS ACTIVATION [18), 19)]

We investigated the conditions for ion implantation and activation annealing aimed at n^+-layer formation. Si as an

n-type dopant was used for doping. First, un- and Mg-doped GaN ([Mg] ~ $1x10^{17}cm^{-3}$) 2 μm in thickness were grown on a sapphire substrate (0001)c by MOCVD. Then, SiO_2 screen oxide 20 nm in thickness was deposited on GaN using a PECVD to suppress any damage or pollution due to ion implantation. Subsequently, Si ion implantation was carried out in four steps in order to adjust the depth profile of Si atoms by 150 nm. The implantation energy levels were 30, 60, 120 and 190 keV. After the screen oxide was removed, 500-nm thick SiO_2 capping layer was deposited. Activation annealing was performed in an Ar ambient by a rapid thermal annealing (RTA), followed by removal of the capping layer. Finally, the Hall measurement was carried out to determine the sheet resistance and sheet carrier density in the ion-implanted layer by the van der Pauw.

Figure 3 shows the results of Hall measurement of GaN after Si ion implantation and activation annealing. It can be seen that the activation ratio (the ratio of sheet carrier density over Si dose) tends to decrease with lower Si doses. This may be attributable to the compensation of donors by the energy level developed by crystalline defects [20]. The activation ratio of the ion-implanted layer formed in the Mg-doped GaN was lower than that in the undoped GaN, probably because activated donors were compensated by the acceptors. The activation ratio of activation annealing at 1260°C for 30 sec was higher than that at 1200°C for 10 sec, indicating that a high thermal budget is needed for activation. As the result, we were successful in obtaining an n^+ layer of sufficiently low resistance with a sheet carrier density of 26 Ω/sq. and a sheet carrier density of approx. $3x10^{15}$ cm^{-2} (activation ratio: 100%), using a Si dose of $3x10^{15}$ cm^{-2}. Moreover, activation was successfully carried out at a low Si dose of some 10^{13} cm^{-2}.

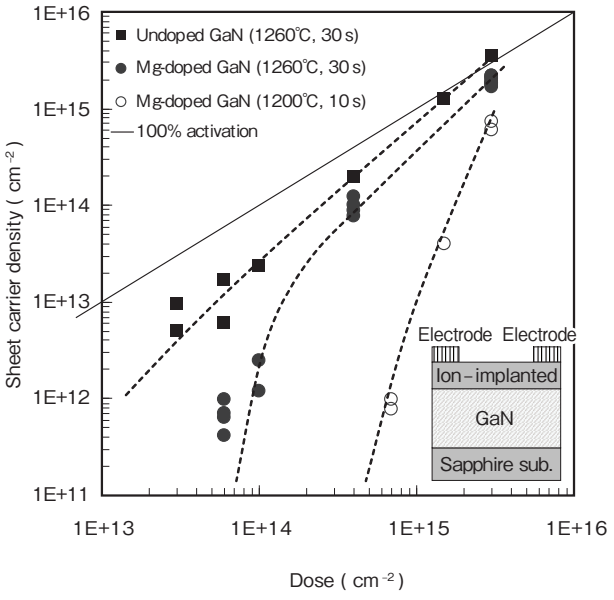

Figure 3 Relationship between sheet carrier density and Si total doses.

4. FABRICATION AND LARGE CURRENT AND HIGH BREAKDOWN VOLTAGE OF GaN MOSFET [21)~24)]

Having successfully formed an SiO_2/GaN with a low-resistance n^+ layer and good interface quality, we proceeded to fabricate GaN MOSFET based on these elemental technologies. Please refer to the literature [25] for the device design, since it is not possible to go into detail here because of space limitations.

First, Mg-doped GaN ([Mg] ~ $1x10^{17}cm^{-3}$) 1 μm in thickness was grown on a sapphire substrate (0001)c by MOCVD. Next, to form n^+ layer, Si ions were implanted into the source and drain regions to a depth of 150 nm with a total dose of $3.0x10^{15}$ cm^{-2}. And, activation annealing was performed in an Ar ambient by an RTA at 1260°C for 30 sec. Next, gate oxide of SiO_2 60 nm in thickness was deposited on the GaN surface by PECVD. After that, annealing was performed in a nitrogen flow in an electric furnace at 900°C for 30 min to reduce the interface states. And, apertures were provided at the source and drain regions by wet etching. After that, source and drain electrodes of Ti/Al were deposited by sputtering, followed by a lift-off process, and annealing was performed in an nitrogen ambient at 600°C for 5 min. The sheet resistance and contact resistance of the n^+ layer were 65 Ω/sq. and $1.9x10^{-7}$ Ωcm^2. Finally, gate electrode of Ti/Au was formed on the gate oxide layer of SiO_2 by sputtering and lift-off.

Figure 4 shows the current-voltage (I-V) characteristics of GaN MOSFET at 250°C. The channel length and width are 4 μm and 16 mm, respectively. In the output characteristics, it has been observed that the drain current changes by the gate voltage and that the drain current

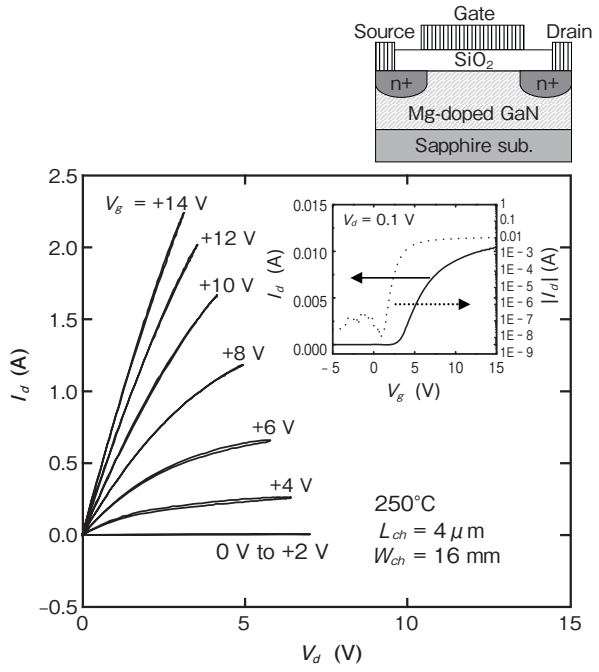

Figure 4 Output characteristics at 250°C of GaN MOSFET with gate width of 16 mm. (Inset: transfer characteristics)

increases and saturates depending on the drain voltage, thus confirming transistor operation. The drain current at a gate voltage of +15 V was more than 2 A. To the best of our knowledge, the operation temperature of 250°C is the highest in the world. Moreover, more than 1-A operation of GaN MOSFET was observed for the first time. In the transfer characteristics, the threshold voltage is +3 V, confirming normally-off operation. Furthermore, the gate voltage at which weak inversion occurs exceeded 0 V; the sub-threshold slope was 328 mV/dec. ; the gate leakage current was lower than 100 nA ; and the On/Off ratio was 10^5.

With this device structure, however, since the electric field concentrates on the drain side end of the gate oxide layer, the breakdown voltage of the transistor is determined by that of SiO_2. As a result, the breakdown voltage is limited to 40 V at the most. In order to disperse the field concentration, field concentration spots are intentionally formed by inserting an n^- layer of REduced SURface Field (RESURF) [26] between the gate and the drain, thereby tilting the electric potential with respect to the n^+ layer. Figure 5 shows the schematics of (a) conventional MOSFET and (b) RESURF-MOSFET, where the RESURF is inserted between the gate and drain electrodes. In the case of conventional MOSFETs, when the gate voltage V_g is lower than the threshold voltage V_{th}, and the drain voltage V_d is extremely high, breakdown occurs in the gate oxide layer near the spot "A" in Figure 5 (a). In the off states, the source and gate are equipotential with the ground, and the resistance of the gate oxide is higher than that of the channel region. For these reasons, almost all the electric field concentrates on the gate oxide, resulting in breakdown near there. In the case of RESURF-MOSFET, on the other hand, the electric field concentrates on the two spots of the gate oxide marked "B" in Figure 5 (b) and the RESURF layer marked "C" in Figure 5 (b); more specifically, field concentration occurs on three spots including the n^-/p junction in the layer thickness direction. Therefore, the electric fields in the gate oxide layer decrease thus increasing the breakdown voltage. We have fabricated GaN RESURF-MOSFETs by using the Si ion implantation technique aforementioned to prepare the RESURF layer.

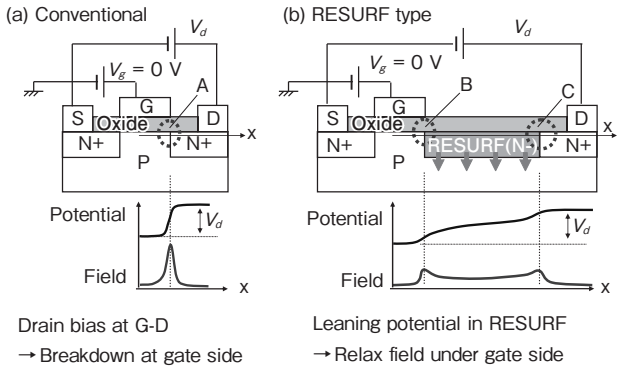

Figure 5 Schematic of potential and field of (a) conventional MOSFET and (b) RESURF-MOSFET.

The Si dose for RESURF layer formation was $6x10^{13}$ cm^{-2}; the sheet resistance and the sheet carrier density after activation annealing were 23 kΩ/sq. and $1.1x10^{12}$ cm^{-2}, respectively; the lengths for the channel and RESURF were 4 μm and 20 μm, respectively; and the gate width was 150 mm.

Figure 6 shows the output characteristics of RESURF-MOSFET. The breakdown voltage was higher than 1550 V, and this value divided by the RESURF length, which is 80 V/μm largely surpasses the critical electric field of Si, which is 30 V/μm. Moreover, the operation current exceeded 2.5 A. This is the first time in the world that a single device of GaN MOSFET has achieved both 1550-V and 2.5-A operations. These results show that this lateral GaN MOSFET can be applied in power switching devices.

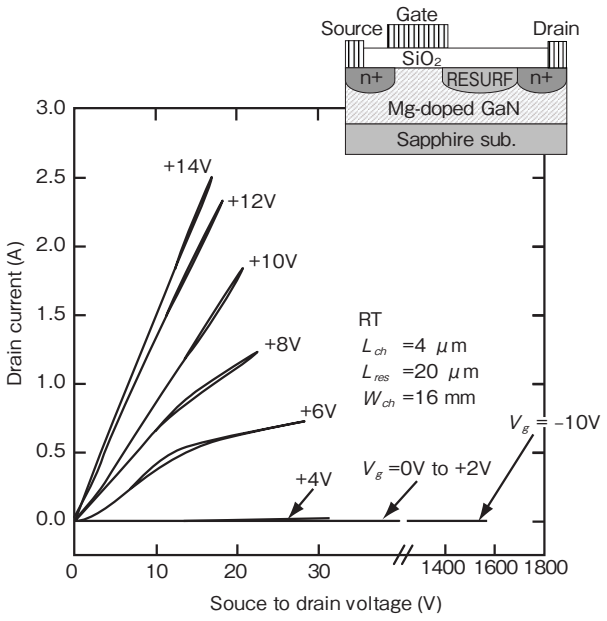

Figure 6 Output characteristics of GaN RESURF-MOSFET.

5. CONCLUSIONS

A GaN-based MOSFET has been developed as a power device to be incorporated in power supply circuits where high-temperature, large-current and high-breakdown voltage operation is required.

Both the formation of n^+ layer and the reduction of SiO_2/GaN interface states were needed for operation of GaN MOSFETs. The n^+ layer was formed by Si ion implantation and activation annealing. Under the conditions of $3x10^{15}$ cm^{-2} in Si ion total dose and of 1260°C for 30 sec in activation annealing, the sheet resistance and sheet carrier density obtained were 26 Ω/sq. and $3x10^{15}$ cm^{-2} (activation ratio: 100%), respectively. Moreover, a high-quality SiO_2/GaN interface was obtained by annealing at 900°C for 30 min. The interface states density calculated by the C-V characteristics at 200°C and the Terman method was lower than $1x10^{11}$ $cm^{-2}eV^{-1}$ ($E_c - E = 0.4$ eV) .

Then a GaN MOSFET was fabricated on a sapphire

substrate (0001)c. The device operation was confirmed at 250°C, the highest temperature in the world. The threshold voltage and the operation current were +3 V and larger than 2 A, respectively. Moreover, a GaN RESURF-MOSFET with higher breakdown voltage was fabricated, achieving the device operation of higher than 1550 V in breakdown voltage and larger than 2.5 A in operation current.

We believe that GaN MOSFETs will find applications in broad fields where high-temperature operation is needed, besides power supplies for automobiles and home appliances.

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