1060 nm VCSEL Array for Optical Interconnection

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ABSTRACT Recently, due to the increase in information volume, optical interconnection is widely spreading in board to board data communication and in other IT equipments. Furthermore, due to increase in information volume, needs for low power consumption version of vertical cavity surface emitting laser (VCSEL) are increasing in data centers and others. Furukawa Electric has achieved the world highest 62% power conversion efficiency in VCSEL, by implementing the double intra-cavity contacted structure to the 1060 nm wavelength chip structure. And, we have confirmed that the VCSEL has sufficient margin in eye-aperture at the 10 Gb/s operation. In addition, we performed reliability test using a total of 3,467 chips, and have verified the random failure at 81FIT per one chip and at 972FIT per 12-channels array. With these test results, the newly developed 1060 nm VCSEL has been evaluated promising satisfactory results as light source for high speed optical inter connection, at which low power consumption is required.

1. INTRODUCTION

Due to the increase of information volume in recent years, needs on low power consumption version of VCSEL, for servers and discrete components in data centers and others, are getting higher. In this circumstance, optical interconnection is attracting attention as a key technology for low power consumption. A parallel multi channel module is adopted for optical interconnection, therefore a low power consumption version on VCSEL is important as a key component of the module. Recently, ultra-high speed performance on VCSEL [1)~4)], with InGaAs strained-layer quantum well in an active layer and with low power consumption performance combined with a C-MOS driver, is reported.

Now, targeting in light source of optical interconnection, we developed the 1060 nm VCSEL array using excellent grade InGaAs/GaAs strained-layer quantum well in an active layer also implementing a double intra-cavity contacted structure in the chip structure.

In this paper, the world highest 62% in power conversion efficiency achievement [5)], 10 Gb/s operation at 12-channels array and reliability test results on total 3,467 chips is reported.

2. Structure of 1060 nm VCSEL

Figure 1 shows a cross sectional pattern diagram of the double intra-cavity contacted type VCSEL with oxidized layer, which we have developed. The layers were grown by molecular beam epitaxy (MBE) method, in which metallic Al, Ga, In were used as group Ⅲ material and thermally cracked As_2 was used as group Ⅴ material. Un-doped AlGaAs/GaAs bottom distributed bragg reflector (DBR), triple layer quantum well active layer (wave length 1060 nm) and AlGaAs oxidized layer were grown by MBE.

Here, we used an elemental Si for n-type and a gas-phased CBr_4 for p-type as a dopant. A contact layer and a current spreading layer were inserted between oxidized layer and top DBR to minimize optical loss from the layers.

After crystal growth, mesa post and oxidized layer were formed. P type and N type of electrodes were formed by the electro-beam evaporator system. Finally, top-DBR was formed, so that the thickness of each layer can be controlled precisely resulting in low optical loss.

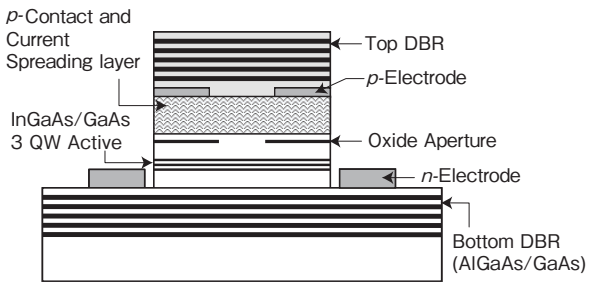

Figure 1 Schematic diagram of 1060 nm VCSEL.

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3. CHARACTERISTICS OF 1060 nm VCSEL

Figure 2 shows the injection current (*I*) vs the light output (*L*) characteristics of the chip with a 7 μm of oxide aperture diameter. Also, the voltage characteristics and the power conversion efficiency (PCF) are shown in the same Figure 2. A reflectance-optimized upper DBR was used for this high output. Then, a threshold current of 0.7 mA and a slope efficiency of 1.0 W/A were obtained. As shown in Figure 2, 62% of the power conversion efficiency was obtained at 5 mA current. As far as we know, this is the highest power conversion efficiency on VCSEL in the world. The power conversion efficiency sustained at 55% for up to 10 mA, and reached 40% even at 90°C. The electric resistance was 50 Ω and the thermal resistance, estimated from the emission wavelength shift value, was 1.8 K/mW. Based on the fitting of *L-I* curves with different numbers of top-DBR pair, the estimated internal loss would be 3cm^{-1} and mirror loss be 22cm^{-1}.

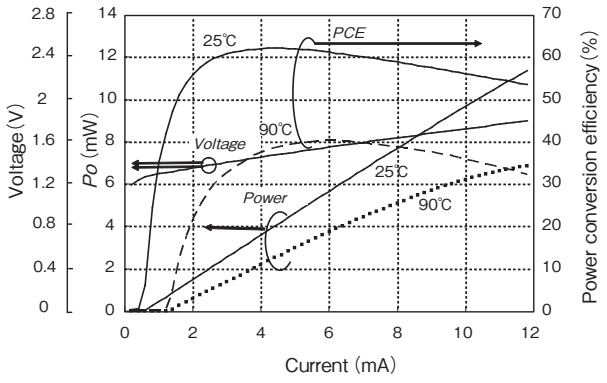

Figure 2 *L-I-V* curve and PCE under 25°C and 90°C.

To realize this 62% of the power conversion efficiency, we followed two different approaches on the double intracavity contacted structure. In the first, the current diffusion layer was set in the cavity. And, the superimposed volume between the current pass with the optical pass was minimized by reducing the electrical resistance. A low optical loss was achieved. For this achievement, the doping density of the current diffusion layer was accurately controlled by paying attention to the standing wave position. In the second, a high Al content DBR was used as a lower DBR. As a result, the low thermal resistance was achieved. Then, the high power conversion efficiency was achieved even at 25 kA/cm^2 of high current density and at 90°C of high temperature.

4. CHARACTERISTICS OF 1060 nm VCSEL ARRAY

Figure 3 shows the current vs the optical output and the current vs the voltage characteristic of a 12-channels VCSEL array. The chip structure was based on the previously explained double intra cavity structure and the reflectance of the top DBR mirror was optimized at 10 Gb/s operation, based on the balance between the threshold current and the slope efficiency. As a result, 0.3 mA at 25°C, 0.8 mA at 90°C of threshold currents were obtained and the slope efficiencies were 0.35 W/A at 25°C and 0.25 W/A at 90°C. The threshold voltage showed almost the same value of 1.15 V at 25°C and at 90°C, and the series resistance was 60 Ω (at 3 mA performance) at these temperatures. The most important feature of the double intra cavity structure, which we adopted, is the small temperature dependency on the current vs the voltage characteristics, in comparison with the commonly used structure in which current is injected through DBR. Another important feature is the low threshold voltage. This is obtained by the adoption of the 1060 nm range, which has a smaller band gap than the commercially supplied common type of 850 nm range. Combining with the driver IC, these features have the possibilities to lower the total power consumption.

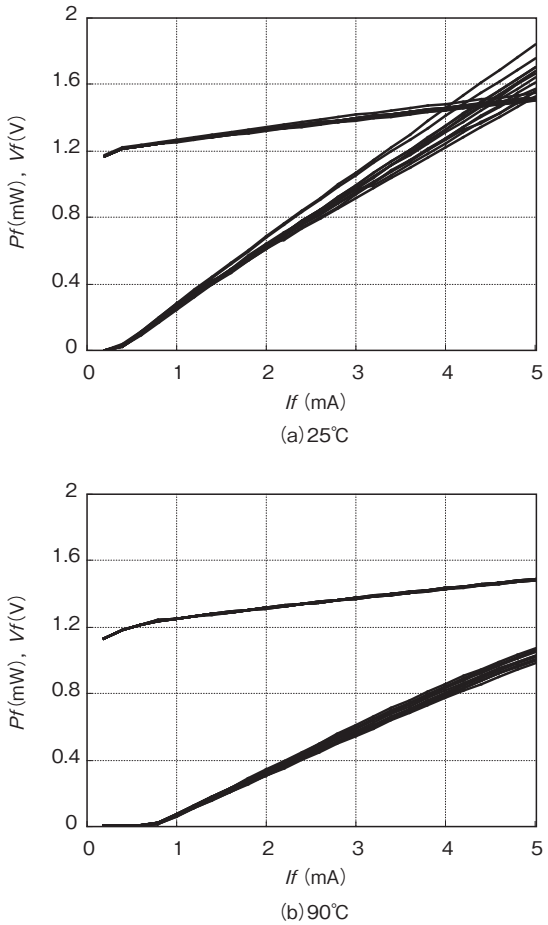

Figure 3 *L-I-V* characteristics of 12 ch VCSEL array

Now, the modulation characteristic at 10 Gb/s is described[7]. A tentative eye pattern example, at 3 mA bias current, is shown in Figure 4. This eye pattern shows that the eye opens properly. The observed rise time and the fall time (tr/tf) at 20%～80% range were 33/41 ps and good margin was obtained against a mask of the 10 GBASE-SR. The degradations of the rise time and the

fall time are estimated at 8 ps and 17 ps, when the input electric signal has 25.2 ps of rise time and 25.6 ps of fall time, in our measurement system.

The low power consumption of 7 mW/Gbps (transmitting and receiving) was achieved on the 10 Gb/s×12 ch parallel multi channel module, which was made up by using the developped VCSEL array[8].

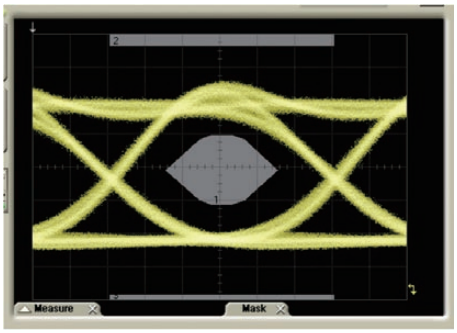

Figure 4 10 Gb/s eye diagram at *Ib*=3 mA

5. RELIABILITY OF 1060 nm VCSEL

Reliability test was performed by mounting VCSEL element into a package for IC (20 pin dial in-line package). All the specimens were treated by burn-in process, before the reliability test and initial failure samples were eliminated. The current vs optical output characteristics and the voltage characteristics were measured at 25°C, every hour, taking specimens out from the oven. The failure criteria was set at 2 dB power degradation time as held in conventional VCSEL aging test.

Table 1 shows the detailed conditions and the results of the reliability test. *Ea*=0.35 eV and n=0 are taken for the random failure calculation, following Telcordia GR-468 standard. Total 3,467 chips were used for this test and degradation was observed in only one chip of the first lot. The cause of this gradation was found out to be the break of the wire which connected the mesa top and the pad electrode in the chip. No degradation was observed after the wiring was improved. The random failure Failure In Term (FIT) number is 81FIT per a chip, which is 972FIT per 12-channels array.

Table 1 Reliability test conditions and test results.

Condition	Quantity (number of chips)	Aging duration (hours)	Device-hours @40°C, 6 mA	Number of failures
70°C, 6 mA	1,026	338–5,736	8.8×10^{6}	1
90°C, 6 mA	1,044	338–5,758	1.6×10^{7}	0
120°C, 6 mA	1,397	400–3,842	2.3×10^{7}	0
Total	3,467		4.78×10^{7}	1

Figure 5 shows the optical output variation of the specimens due to aging when tested at 90°C, 6 mA and 120°C, 6 mA[7]. From these test results, no gradual degradation was observed and the long time stability was confirmed. In addition, not only optical output but also threshold current did not show noteworthy variation, and no wear out failure was observed in this test.

From reliability point of view, as well, these test results show the superiority of 1060 nm range VCSEL, in which the active layer consist of InGaAs/GaAs without Al.

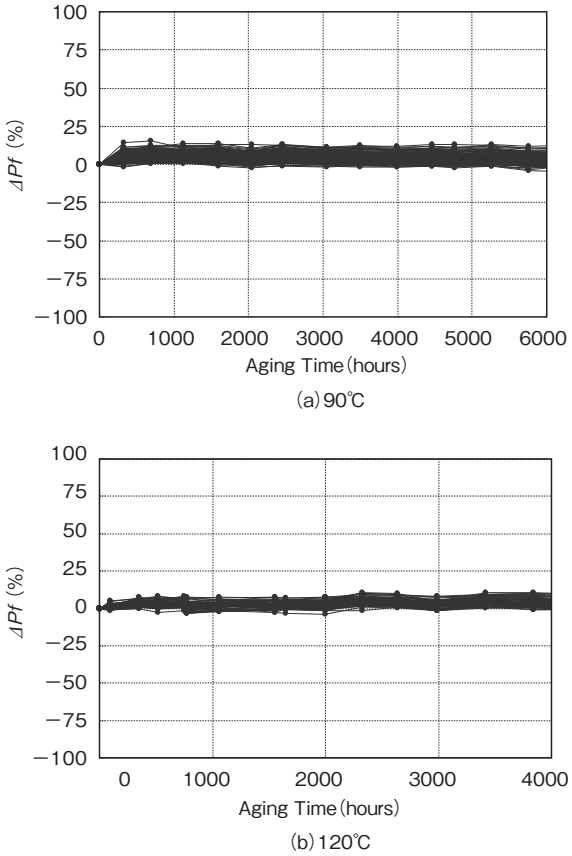

Figure 5 Output power variation in aging test. (at 6 mA, 25°C)

6. IN CONCLUSION

The world highest power conversion efficiency of 62%, was achieved with the high output corresponding designed construction, by adopting the double intra-cavity contacted structure in 1060 nm range VCSEL. Furthermore, a 10 Gb/s operation with sufficient eye aperture margin was confirmed in the 10 Gb/s operation optimized 12-channels array. Also a 81FIT per chip in random failure FIT number, and a 972FIT per 12-channels array were verified by the reliability test with a total 3,467 chips. From these test results, the developed 1060 nm VCSEL has a promising future as a light source for high speed optical inter connection in which a low power consumption is required.

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