Development of Flexible Bumped Tape Interposer

*by Kazuhito Hikasa [*], Toshiaki Amano [*], Toshiya Hikami [*], Ken'ichi Sugahara [*] and Naoyuki Toyoda [*2]*

ABSTRACT Recently electronic equipment have remarkably been improved becoming lighter and more compact and having upgraded functions, requiring electronic components mounted thereon to have more pins, smaller pitches, and smaller mounting spaces. Thus chip size package (CSP) has become the mainstream of packages for chip-sized electronic components. In response to such situations, the authors have developed a flexible bumped tape interposer (FBTI) with solder bumps for flip-chip processing of CSPs. The vias of this interposer are filled with metals such as Cu or solder, and chips are mounted by flip-chip bonding the SnAg-solder bumps with the Au stud bumps on Si chips. Consequently, this interposer can cope with such requirements as higher frequencies, elimination of Pb, and higher bonding reliability. This paper reports on the structure, manufacturing process, features, results of prototype manufacturing, reliability, and application examples of this interposer.

1. INTRODUCTION

Recently the development of electronic equipment represented by mobile phones, PDA (Personal Digital Assistance), and notebook PCs is quite remarkable becoming lighter and more compact and having upgraded functions, requiring electronic components mounted thereon to have more pins, smaller pitches, and smaller mounting spaces as well as better high-frequency performance.

Accordingly, electronic devices are experiencing innovative improvements including, e.g., the development of wafer-scale chip size packages (CSPs) and new packages of chip-stacking type.

Semiconductor chip mounting methods for these devices come in two types: wire-bonding process and flip-chip process with face-down mounting. Whereas the flip-chip process using solder bumps is a superior method with smaller mounting spaces, more pin counts, better high-frequency performance, and higher reliability, the wire-bonding process is a matured technology with lower costs than the flip-chip process, and thus is widely used. It is probably because of this advantage that the wire-bonding allegedly accounts for mounting of about 90 % of all the semiconductor devices, and the flip-chip process is not widely used yet as a multipurpose technology.

However, it is thought that when the devices become lighter and more compact with better high-frequency performance in future, the wire-bonding technology may reach a limit thus requiring wider use of flip-chip process. To implement this technology as a low-cost and easy-to-use mounting method, a new interposer is necessary. Therefore, we have developed, through application of Furukawa Electric's proprietary technology of solder plating, a flexible bumped tape interposer (FBTI) with solder bumps for flip-chip processing of CSPs.

2. STRUCTURE OF INTERPOSER

2.1 Polyimide Substrate

The structure of a newly developed interposer using polyimide substrates is described below. Figure 1 shows the appearance of an interposer using a polyimide substrate 40 μm in thickness, and Figure 2 shows its enlarged illustration.

The side with bumps shown in Figure 1 (hereafter called “E-side”) is to be mounted with chips, on which SnAg-solder bumps 10~25 μm thick and 75 μm square are formed at 150 μm intervals. The wiring uses 18 μm thick Cu foil spaced at a minimum pattern gap of 75 μm.

Meanwhile, the structure has a via side (hereafter called “BC-side”) of LGA (Land Grid Array) with vias spaced at 0.5 mm intervals filled with SnAg solder.

[*] Components and Advanced Interconnect Technologies Dept., Ecology & Energy Lab.

[*2] Engineering Sec., Electronic Components Dept., Electronic Components Div.

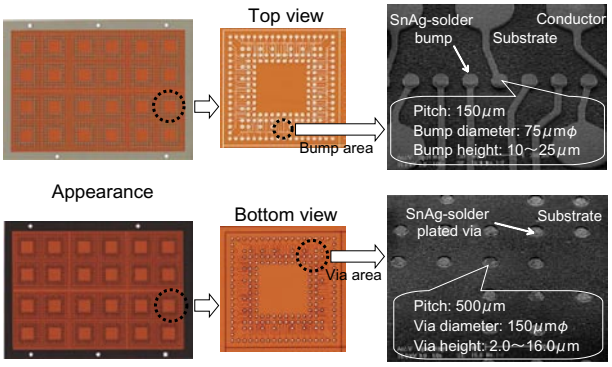


Figure 1 Appearance of interposer using 40 μm-thick polyimide substrate.

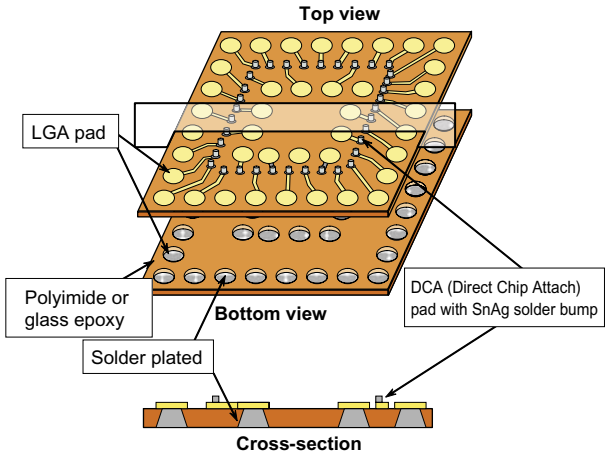


Figure 2 Illustrative drawing of interposer shown in Figure 1.

2.2 Glass Epoxy Substrate

Although not illustrated specifically, an alternative structure using a glass epoxy substrate 50 μm thick is available, on the E-side of which, like the polyimide substrate, SnAg-solder bumps 50 μm square minimum are formed at minimum intervals of 84 μm. The wiring uses 18 μm thick Cu foil spaced at a minimum pattern gap of 34 μm. Moreover, also available are the structures with NiAu plating for the test terminals or with anti-oxidation Sn plating for the Cu foil surface.

The BC-side of these structures has an LGA with vias 150 μm square and spaced at 0.35 μm intervals, plated with SnAg solder thicker than for the substrate .

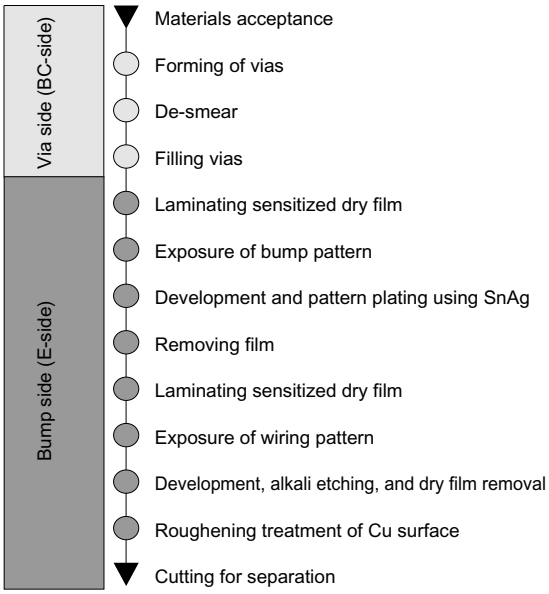
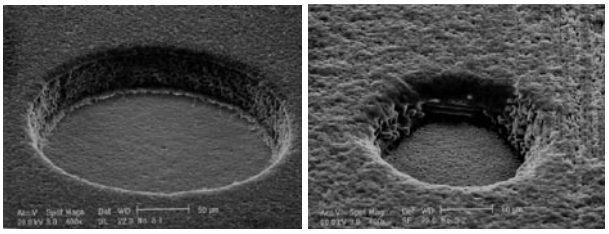


Figure 3 Manufacturing process.



a) 40 μm-thick polyimide b) 50 μm-thick glass epoxy

Figure 4 Appearance of vias after laser-perforation and de-smearing.

3. MANUFACTURING PROCESS [1)]

Figure 3 illustrates the manufacturing process of interposers.

The BS-side is processed first.

1) Vias are formed using CO_2 laser beam
2) Removal of laser smear (De-smear)
3) Vias are filled using SnAg-solder electroplating (Via-filling)

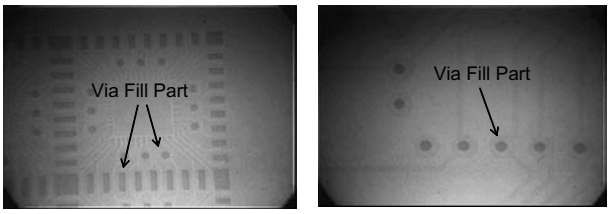
   Next, the E-side is processed.
4) Sensitized dry film is laminated onto the Cu foil surface
5) Exposure using glass mask to form solder bumps
6) Development and SnAg-solder electroplating of bumps
7) Removal of dry film
8) Sensitized dry film is laminated onto the Cu foil surface
9) Exposure using glass mask to form solder bumps
10) Development, alkali etching, and dry film removal
11) Roughening of Cu surface aimed at improving adhesion force with NCF (Non Conductive Film), adhesive, and under-fill
12) Cutting for separation

4. FEATURES

Representative features of the interposer developed here are described below.

4.1 Neatly Perforated Vias

Because CO_2 laser beam capable of micro-fabrication is used to perforate the vias, perforation with high positional accuracy is achieved. Figure 4 shows the vias on a 40 μm-thick polyimide and a 50 μm-thick glass epoxy, respectively, after they are laser-perforated and de-smeared. It can be seen that there are no residuals around the vias after de-smearing.



a) 40 μm-thick polyimide b) 50 μm-thick glass epoxy

Figure 5 Soft X-ray images of via-filling.

4.2 Neatly Filled Vias

Because the vias are optimally de-smeared after laser perforation exposing genuine Cu surface, they are neatly filled with SnAg solder or Cu plating.

Being also capable of responding to Pb-free processes, the vias are void-free and have small electrical resistance, thus achieving via bonding of higher reliability in comparison to the conventional via-filling using electrically conductive paste or solder paste. Figure 5 shows soft X-ray images of vias, indicating void-free via-filling.

4.3 Capable of Responding to Flip-Chip Bonding of High Reliability

The interposer has Pb-free bumps of SnAg solder for flip-chip bonding process. Flip-chip bonding based on Au stud and SnAg-solder bumps can respond to high-frequency components, demonstrating high reliability.

4.4 Availability of Various Substrates

With regard to the substrate, organic materials such as polyimide and glass epoxy are available, with the thickness not more than 50 μm. Table 1 shows the material properties used in the current development.

Because thin and flexible materials are used for the substrate, the chip bonding areas and the mother-board bonding areas have high reliability. Moreover, the two types of substrates are applicable to the same production line.

4.5 Superior Adhesion with Encapsulating Resin

The Cu foil surface undergoes roughening treatment so as to improve the adhesion force with NCFs, adhesive, and under-fill, significantly enhancing the reliability of packages. See Figure 6.

5. RESULTS OF EXPERIMENTAL MANUFACTURE

We have intently investigated the conditions for via-filling plating and SnAg-solder plating of bumps --these elements constitute the major features of the interposer developed here-- including the plating solution, plating conditions such as current density and time, and the type and the position of plating electrodes. Below will be reported the results of the experimental manufacture such as the generation of intermetallic compound layer, metallographic structures, the height of plating, and the composition of Ag.

Table 1 Properties of materials used for the interposer developed here.

Item		Unit	Polyimide	Glass epoxy	Test method
Thickness		mm	0.04	0.05	
Volume resistance		Ω·cm		5×10^{15}	IPC-TM-650, 2.5.17
Surface resistance		Ω		5×10^{14}	
Insulation resistance		Ω	4×10^{13}	5×10^{13}	IPC-TM-650, 2.5.9
Heat resistance of solder			260°C×60 sec. Passed	260°C×120 sec. Passed	
Peel strength		N/cm	17.0	14.7	JIS C-5012
Flexual strength	25°C	MPa	271	520	IPC-TM-650, 2.4.19
	150°C			140	
Elongation at break point		%	56.0		
Modulus of elasticity	25°C	MPa	4500	10000	
	150°C			9100	
	200°C			3000	
Ratio of size variation after etching	MD	%	0.00		
	TD	%	-0.04		
Ratio of size variation after heating	MD	%	-0.04		250°C×30 min
	TD	%	-0.04		
Heat resistance in oven				OK	260°C×60 min
T_g		°C		180	
Water absorption		%		0.31	
UL flame class			UL-94V-0	UL-94V-0	

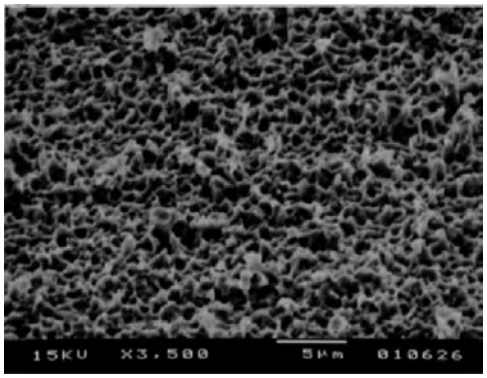


Figure 6 Cu foil surface after roughening treatment.

5.1 Generation of Intermetallic Compound Layer

Figure 7 shows an FIB-SIMS (Focused Ion Beam-Secondary Ion Microscope) image at an angle of 45° of the interface between the Cu foil and SnAg solder after plating. The generation of a thin and uniform intermetallic compound layer can be observed, proving superior plated conditions with metallic bonding.

5.2 Metallographic Structures

Figure 8 shows a 45° FIB-SIMS image of Ag structure after SnAg plating. The Ag grain is seen to be small in size and dense in structure, demonstrating that the SnAg solder has excellent properties as a soldering material.

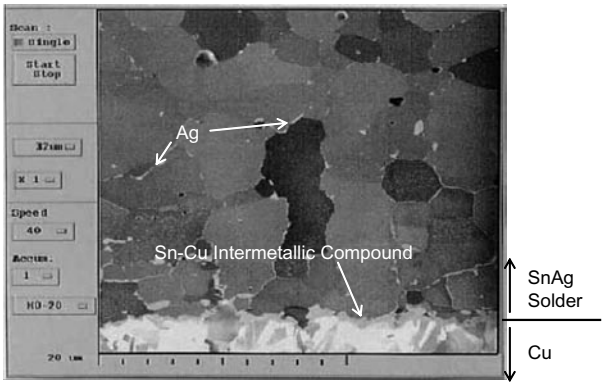


Figure 7 FIB-SIM image of the interface between Cu and SnAg-solder plating.

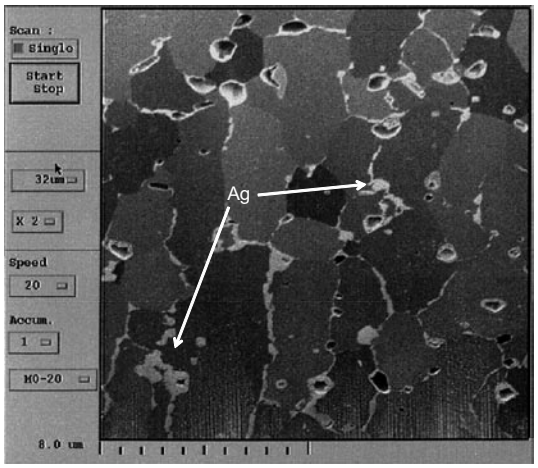


Figure 8 FIB-SIM image of SnAg-solder plating.

5.3 Height of Plating

The height of plating was measured using a focal depth meter. The polyimide substrate samples were measured using 15 lots and at 60 points randomly chosen per one lot, defining a 100-m long, 250-mm broad roll as one lot. The glass epoxy substrate samples were measured also using 15 lots and at 108 points randomly chosen per one lot, defining a 150-m long, 250-mm broad roll as one lot. The statistical results are shown in Table 2. Although the variations of bump heights and via heights are within a level that causes no practical problems in bonding, we intend to reduce both of the standard deviations to not more than 1.5 μm in future.

5.4 Ag Composition

The Ag composition of solder was measured using EPMA (Electron Probe Micro Analysis). Measurements were made using 15 lots and at nine points per one lot, defining a 100-m long, 250-mm broad roll as one lot for the polyimide substrate and a 150-m long, 250-mm broad roll as one lot for the glass epoxy substrate, respectively. The statistical results are shown in Table 3. It can be seen that the Ag composition is stabilized in terms of both via plating and bump plating.

Table 2 Statistics of bump height and via height in solder plating.

	Material	Polyimide film	Glass epoxy
Bump height (μm)	MAX	20.5	15.0
	MIN	10.5	5.0
	AVE	15.2	8.5
	STD	1.7	1.8
Via height (μm)	MAX	20.0	16.0
	MIN	-4.0	2.0
	AVE	8.3	9.3
	STD	5.3	3.1

Table 3 Statistics of Ag composition in solder plating.

	Material	Polyimide film	Glass epoxy
Bump (Ag wt%)	MAX	3.94	3.96
	MIN	1.52	1.39
	AVE	2.79	2.16
	STD	0.67	0.57
Via (Ag wt%)	MAX	3.66	4.16
	MIN	1.53	1.39
	AVE	2.00	2.42
	STD	0.52	0.54

6. RELIABILITY

The basic reliability of the interposer developed here was evaluated, and the results will be reported below.

Si chips were flip-chip bonded on the polyimide-substrate interposer, followed by molding to make package samples, which were subsequently solder-bonded with a mother-board to make mother-board samples. Reliability was evaluated for the two types of samples.

6.1 Preparation of Samples for Reliability Evaluation

6.1.1 Packaging

Figure 9 shows the sample preparation process for reliability evaluation. First, Au stud bumps are formed on the electrode side of Si chips, while Nagase-Chiba URF200 is supplied onto the interposer, near the center of an area where a Si chip is mounted. Post flux (Harima Chemical's F-50F, without cleaning flux) is painted on the Au stud bumps, and is post-cured at 150°C for 5 min. The Si chips are solder-bonded at 250°C for 10 sec using the gang-bonding method with heating tools. After bonding, under-fill (NAMICS U8437-2) is filled in and cured at 150 °C for 20 min, thus encapsulating the interposer into a package.

6.1.2 Mounting of Package

The package above mentioned is mounted on the mother-board as described below.

The mother-board was prepared using a 1.6-mm thick

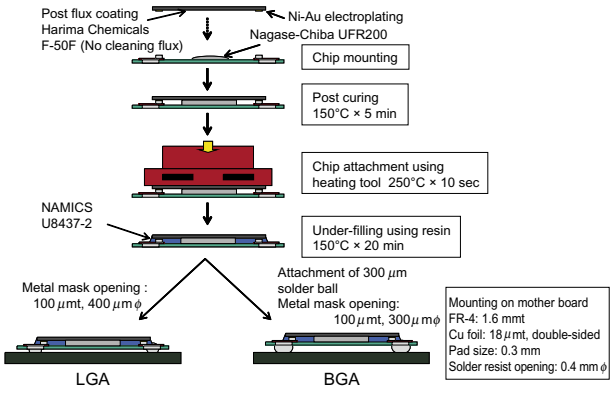


Figure 9 Sample preparation process for reliability evaluation.

FR-4 substrate, 18 μm-thick Cu foil, 0.3-mmϕ electrodes, and 0.4-mmϕ solder resist openings; and two verification levels of solder-bonding samples were set up assuming LGA package and BGA (Ball Grid Array) package.

The LGA package sample was fabricated by solder-bonding using a metal mask for solder paste supply having 400 μmϕ openings and a 100 μm thickness. The BGA package sample was fabricated by solder-bonding the package having 300 μmϕ solder balls on its electrode side using a metal mask for solder paste supply having 300 μmϕ openings and a 100 μm thickness.

6.2 Contents of Reliability Tests

Basic reliability tests were conducted over three verification levels of package alone, LGA-simulating mother-board mounting, and BGA-simulating mother-board mounting, using 20 samples for each level.

The packages alone were evaluated using stylus method to determine whether or not there was conduction between the BGA lands. As for the LGA and BGA, the electrical resistance between the test pads was measured using four-terminal method. The monitoring limits were set to 1 mΩ and 1000 Ω, and the pads with a resistance exceeding the upper limit were counted as a fracture. Moreover, for the purpose of confirmation, bonding areas were cross-sectionally polished and visually examined for occurrence of cracks.

As a result, all the samples prepared at this time passed the reliability tests as shown in Table 4, demonstrating excellent reliability.

7. APPLICATION EXAMPLES OF INTERPOSER

Application examples of the interposer developed here will be presented below. All of them have been adopted by Toshiba Semiconductor Company.

7.1 TQON (Thin Quad Outline Non-leaded)

Figure 10 shows the appearance of a TQON using a polyimide substrate, and Figure 11 illustrates the structure. The TQON features compact size, low profile,

Table 4 Conditions and results of reliability tests.

Test item	Test condition	Pass criteria	Failure rate		
			(1) Component BGA	On the board (2) LGA	On the board (3) BGA
Thermal shock	-55 to 125°C 5 min. dwells	<1 % Failure probability	>2000 cycles 0/20	288 cycles 0/20	547 cycles 0/20
High temp. high humid.	85°C, 85 % RH, no bias	Zero or one failure in 168 hours	0/20	—	0/20
Autoclave	121°C, 100 % RH	24 hours	0/20	—	0/20
High temp. storage	150°C	1008 hours	0/20	—	0/20
Pre-conditioning JEDEC	85°C, 85 % RH, 168 hours 220°C reflow 3 pass	Level 1	Level 1 passed	—	—

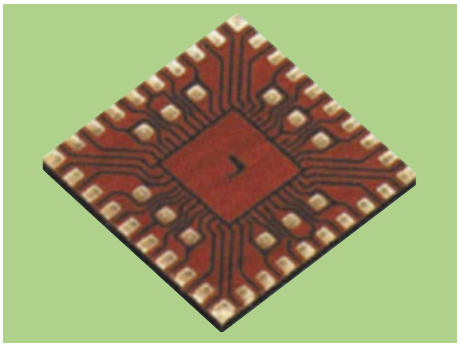


Figure 10 Appearance of TQON.

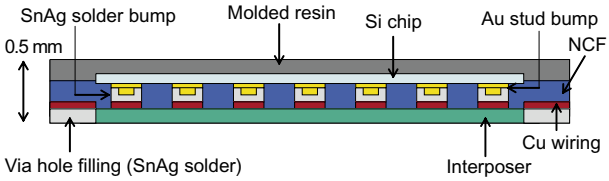


Figure 11 Illustrative drawing of TQON.

and lightweight, and are mainly used for mobile equipment such as mobile phones. Its lead count ranges 16~48 pins; the lead pitches are 0.5 mm and 0.5 mm/0.65 mm for the peripheral type and the area type, respectively; the height is 0.5 mm; and chips are flip-chip bonded on the one side while the other side is molded.

7.2 PTP (Paper Thin Package)

Figure 12 shows an SMB (System Block Module) comprising stacked PTP of glass epoxy substrate. PTP refers to a low-profile packaging technology to implement IC cards with 50-μm chips mounted on a glass epoxy substrate as well as three-dimensional mounting of multi-chips. The SMB shown in Figure 13 has a structure constituted of multi-stacked PTPs, and it has the potential of integrating, by stacking, most of the circuits for a mobile phone into one package.

TQON and PTP are used for packaging in the area of

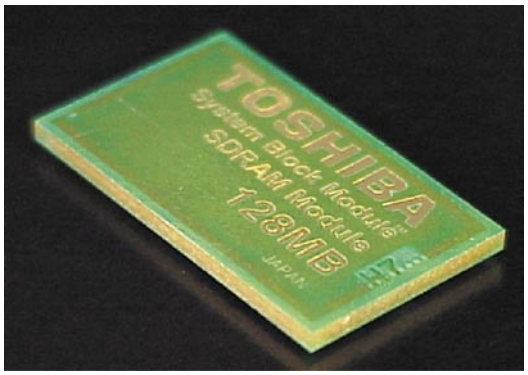


Figure 12 Appearance of SBM.

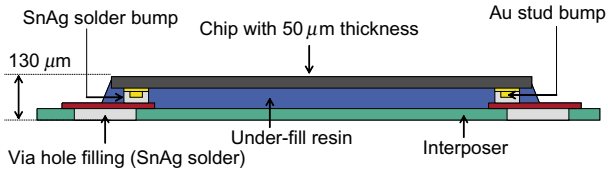


Figure 13 Illustrative drawing of SBM.

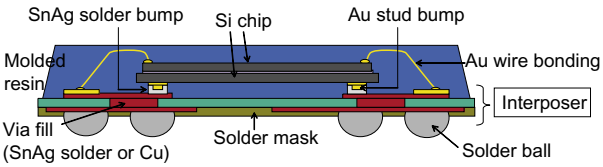


Figure 14 Interposer under development.

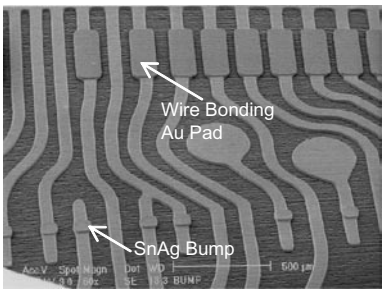


Figure 15 SEM image of bump side of the interposer shown in Figure 14.

electronic equipment such as mobile equipment including mobile phones, where lighter and more compact products are required together with advanced functions and high speed, demonstrating the advantages of flip-chip mounting processes.

7.3 New Product under Development

Figure 14 shows an interposer under development. This is a two-layered interposer, the bump side of which is provided with SnAg-solder bumps for flip-chip bonding and an Au-plated land for wire-bonding (the SEM photo is shown in Figure 15), and the layers are bonded together after the vias are filled using Cu plating. Furthermore, two chips can be flip-chip bonded and wire-bonded respectively to form a stack-bonded structure. Use of this interposer permits mounting of multiple chips in one package, thereby responding to the requirement for packages of higher performance.

8. IN CONCLUSION

We have developed, by forming SnAg-solder bumps which have high bonding reliability with Au stud bumps and by satisfactorily via-filling, an entirely new interposer for CSP that is compatible with Pb-free processes. The product has been adopted by Toshiba Semiconductor Company. We believe that the use of this interposer makes the flip-chip bonding process a cost-effective technology, thus helps our customers to promote the development of new products that are lighter and more compact, and have advanced functions and high speed.

ACKNOWLEDGEMENT

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